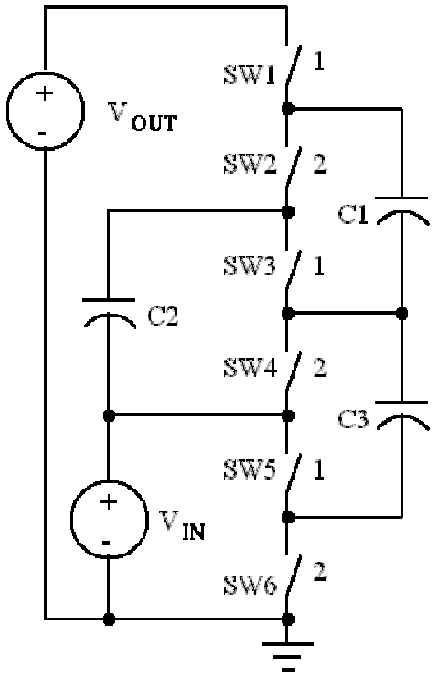
Integrated Power Conversion – The Switched Capacitor Approach

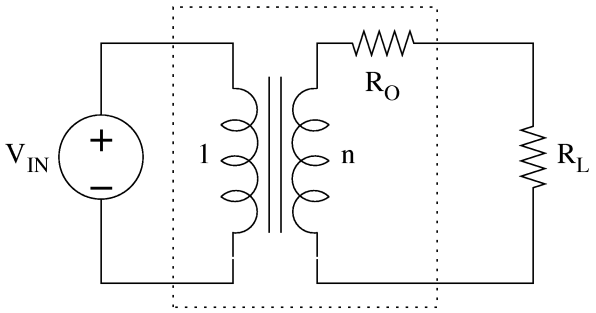
Profs. Seth Sanders and Elad Alon

Vincent Ng, Hanh-Phuc Le, and Mervin John
EECS Department, UC Berkeley

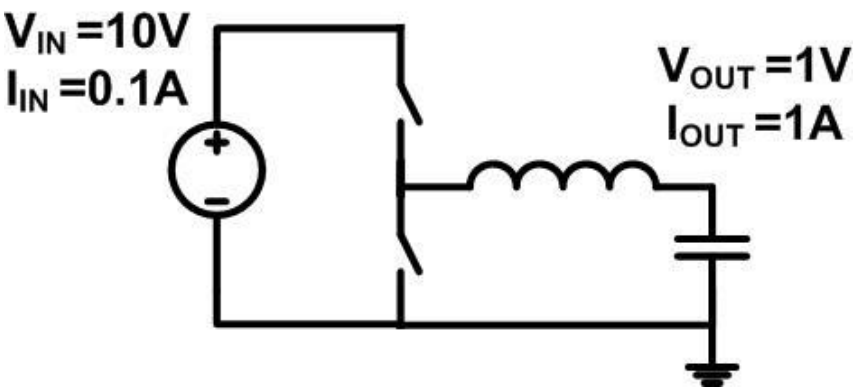
Switched Capacitor Power Converters

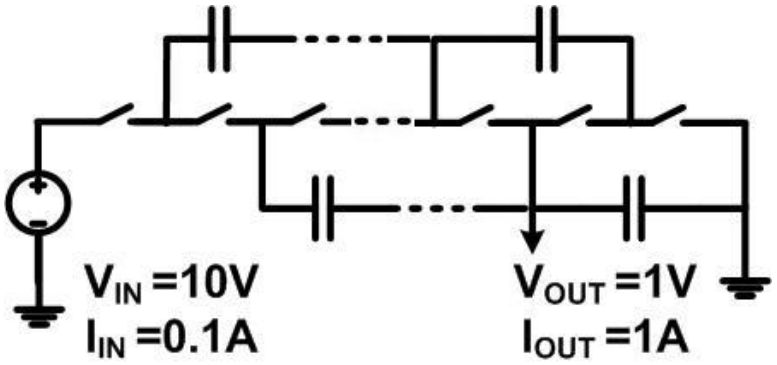
- Only switches and capacitors
- Can support multiple input or output voltages/terminals
- Simple full integration in standard process
- Works well over a wide power range
  - Single mode, can adjust clock rate
  - No minimum load
- No inductive switching losses
- Stacked devices enable high voltage with low voltage processes
- Simple low freq model as an ideal transformer with Thevenin impedance
  - freq dependent loss and leakage





First Look





Magnetic boost/buck:

- 10-to-1 V conversion, 1A @ 1V
- S1,S2 rated for V-A product of V*I = 10 V-A
- Sum up to 20 V-A
- Need inductor, inductor loss, Inductive switching

10-to-1 Ladder Switched-Cap:

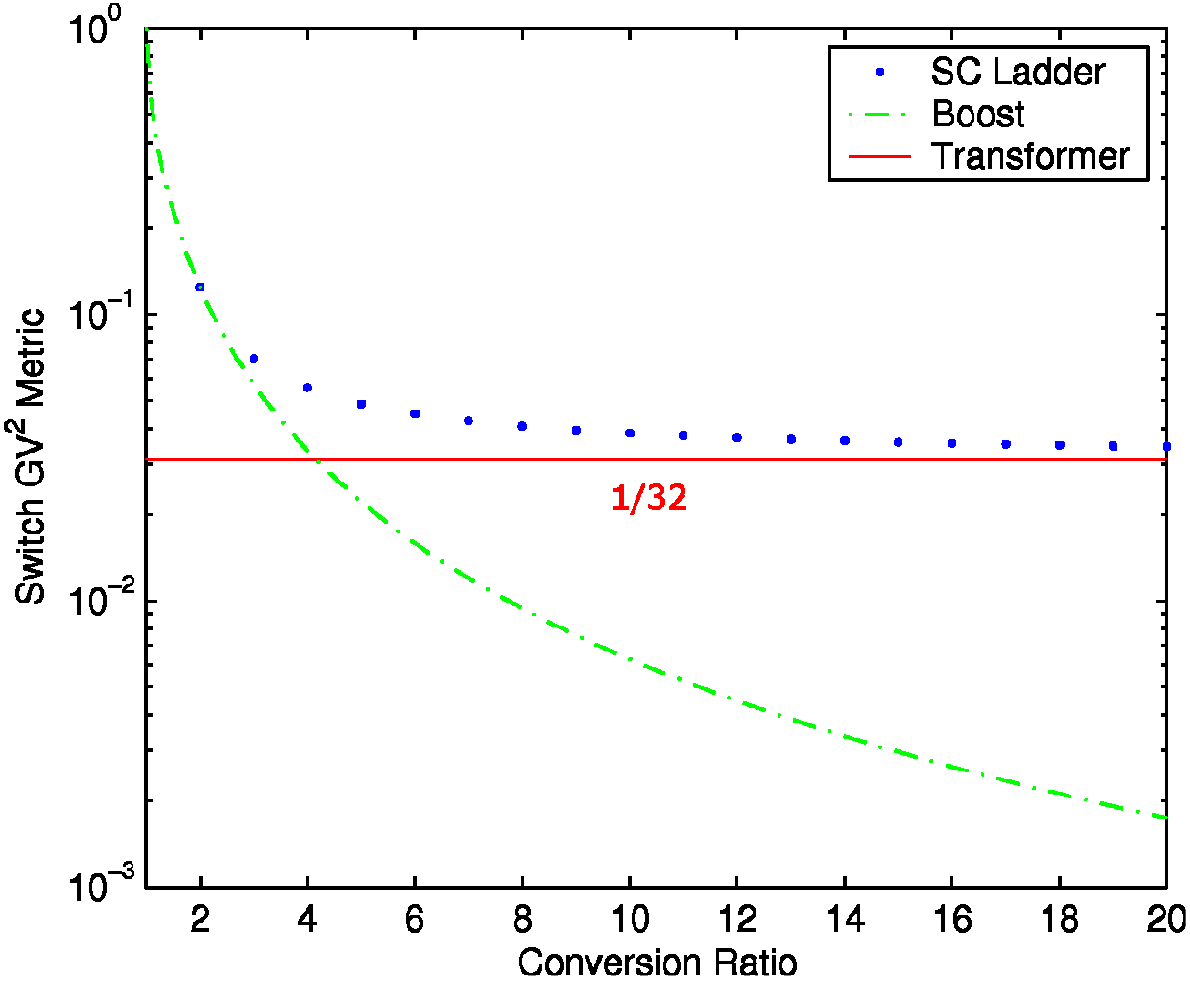
- 10-to-1 V conversion, 1A@1V
- 20 switches, each blocks 1V
- 18 switches handle 1/5 A
- 2 switches handle 9/5 A
- V-A product sums up to 36/5 =7.2 V-A
- Intrinsic CMOS device convenient

Conduction Loss Comparison

M. Seeman, S. Sanders, IEEE T-PELS, March 2008

•Performance compared with switch GV² metric:

$$\frac{G_{OUT}V_{OUT}^2}{\sum G_i v_{r,i(rated)}^2}$$



•Since converters are bi-directional, graph applies equally to step-down converters

•Magnetic components modeled with *zero* conduction loss, and *no* switching loss impact

Reactive Components

- **Fundamental Constraint on dc-dc's:**
  - **Power scales with energy storage, parameterized by conversion ratio and ripple**

- **Buck:**

$$\frac{P}{f_s E_L} = \frac{4}{1-D} \bullet \frac{R_L}{(1+R_L)^2} = 4\frac{G}{G-1} \bullet \frac{R_L}{(1+R_L)^2}$$

  - R_L **current ripple ratio**
  - **G is current or voltage gain**
  - **Analogous constraint on input cap**
  - **Need cap at output for bypass**
  - **Buck is "efficient" topology – i.e. it has minimally rated inductor**

(Kassakian et al, 1991 text)

- **Example: 2-to-1 V @ 1A; f = 250 MHz**
  - **3 turn 500 *um* diam spiral inductor in *25 um* thick Cu with 25 *um* width and spacing: ~2.5 nH with ~100 mohm dc resistance**
    - $R_L = 0.4$
    - **10 nJ/sq.mm peak**
    - **Eat at least 10% conduction loss.**
  - **No accounting for ac resistance, substrate loss, interconnect to this superlevel, nor inductive switching loss**

Switched Cap

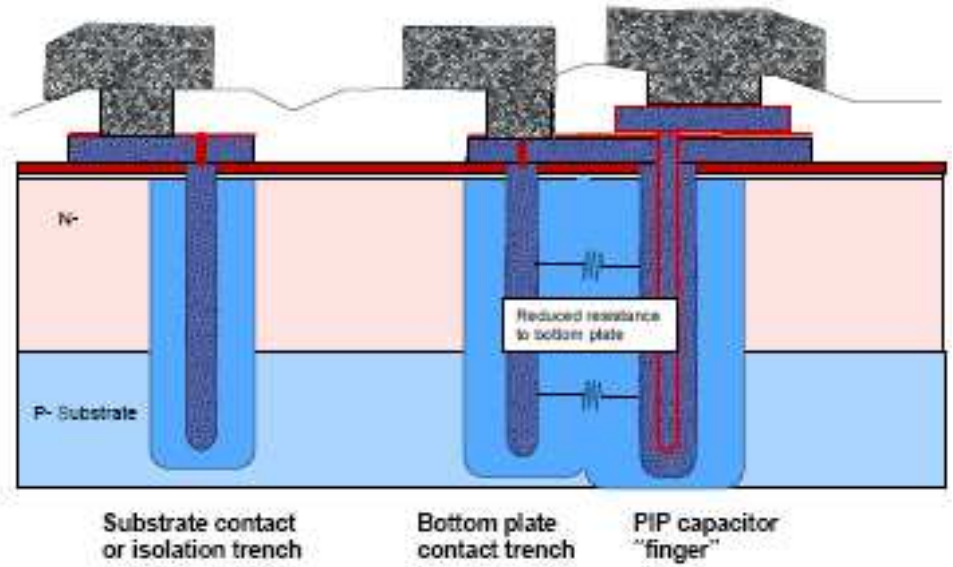
- Fundamental constraint on caps in S-C ckt analogous to that on L,C in buck
- Series-parallel topologies are “efficient” in utilization of cap energy
- Ladder & Dickson not too bad
- Voltage swing (ripple) amounts to charge sharing loss
- Caps:
  - M-I-M and Gate Cap: 5-10 nF/sq.mm @ 2 V: 20-40 nJ/sq.mm
  - Deep trench cap: 200-800 nF/sq.mm: 2 uJ/sq.mm, with 100’s MHz ESR corner

“A LOW SERIES RESISTANCE, HIGH DENSITY, TRENCH CAPACITOR FOR HIGH-FREQUENCY APPLICATIONS,”

G. Grivna, S. Shastri, Y. Wu, & W. Cai, PwrSoC 2008, Sept. 2008, Cork

Similar work by others, eg. IPDIA

X-section drawing of “wrap-around” PIP capacitor in lightly doped substrate



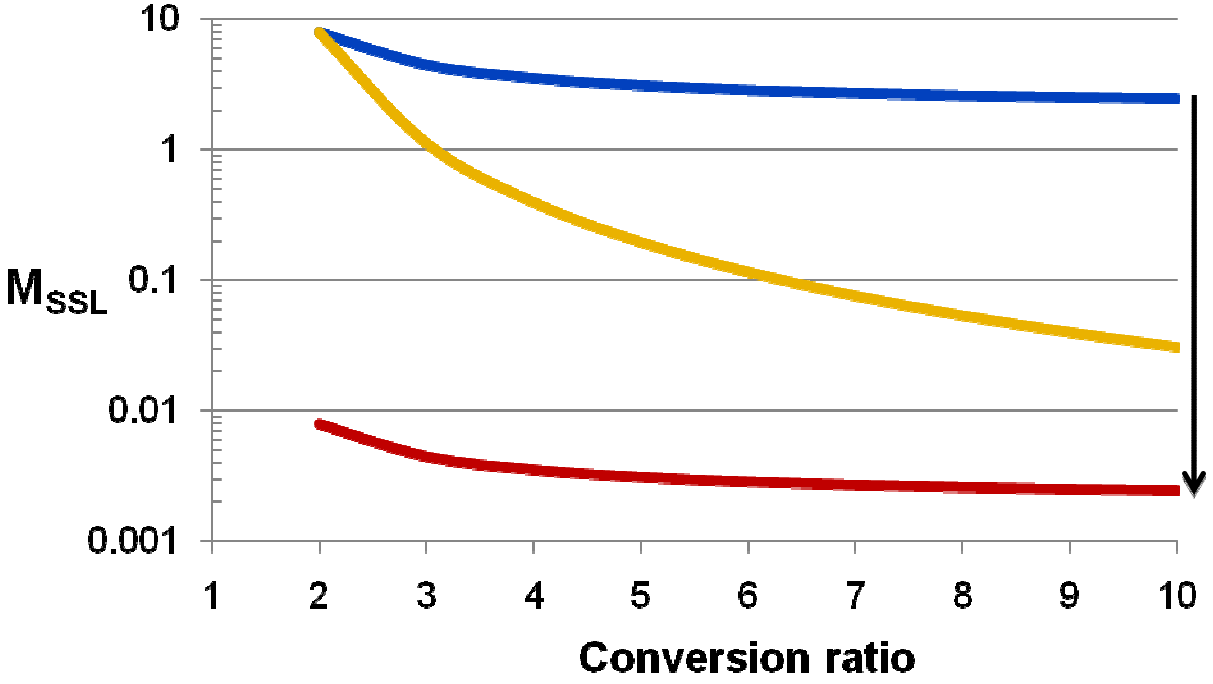
Discrete Inductors vs. Discrete Capacitors

Type	Manufacturer	Capacitance	Dimension	Energy Density
Ceramic Cap	Taiyo-Yuden	22µF @4V	1.6 x 0.8 x 0.8	**344**
Ceramic Cap	Taiyo-Yuden	1µF@35V	1.6 x 0.8 x 0.8	**1196**
Tantalum Cap	Vishay	10µF@4V	1.0 x 0.5 x 0.6	**533**
Tantalum Cap	Vishay	100µF@6.3V	2.4 x 1.45 x 1.1	**1037**
Electrolytic Cap	Kemet	22µF@16V	7.3 x 4.3 x 1.9	**94**
Electrolytic Cap	C.D.E	210mF@50V	76φ x 219	**172**
Shielded SMT Inductor	Coilcraft	10µH @ 0.21A	2.6 x 2.1 x 1.8	**0.045**
Shielded SMT Inductor	Coilcraft	100µH @ 0.1A	3.4 x 3.0 x 2.0	**0.049**
Shielded inductor	Coilcraft	170µH @ 1.0A	11 x 11 x 9.5	**0.148**
Shielded inductor	Murata	1 mH @ 2.4A	29.8φ x 21.8	**0.189**

>1000x

- Capacitors have >1000x higher energy density than inductors

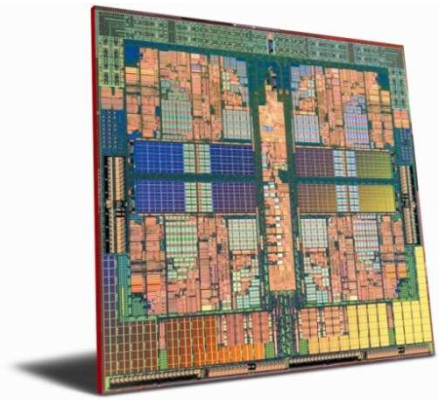
Reactives comparison



$$M_{SSL} = \frac{I_{OUT}^2 V_{OUT}^2}{\left(\sum_{i \in caps} \left| i_{c,i} v_{c,i(rated)} \right|\right)^2}$$

- Derate inductor by 1000 X
- Explains superior reactive element usage in discrete cap example

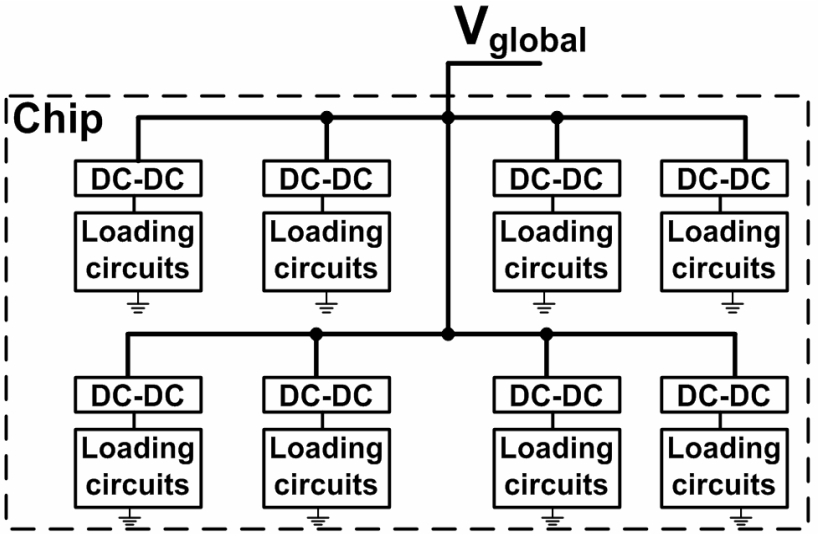
Ex. 1: Multi-Core On-Die VR Motivation – Power Reduction



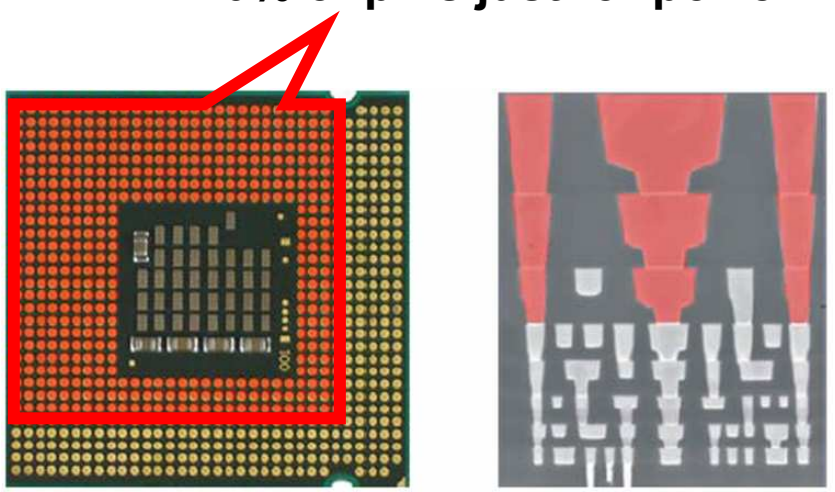
AMD Phenom Quad Core Processor

- **Clear need for separate supplies to enable per-core power management.**

How to efficiently support multiple voltage rails on the die?



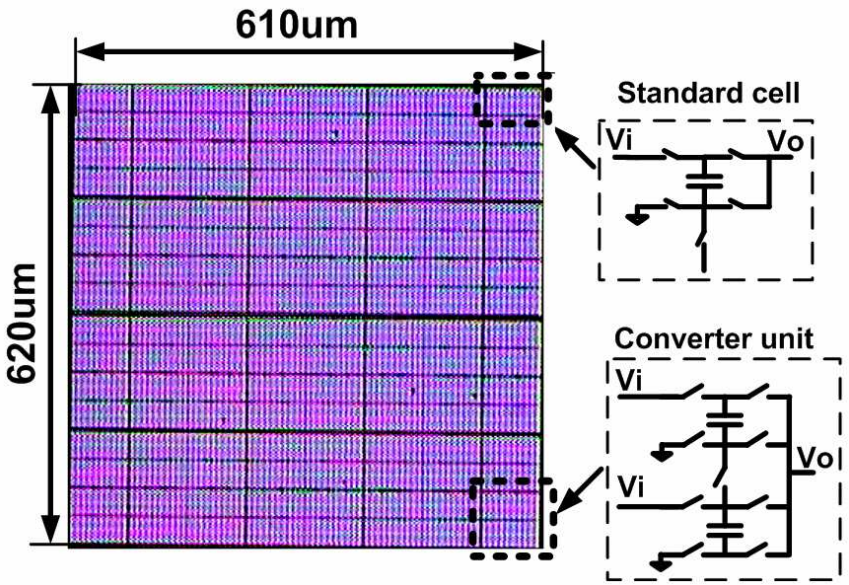
70% of pins just for power



100W - 1V - 100A - 1mΩ

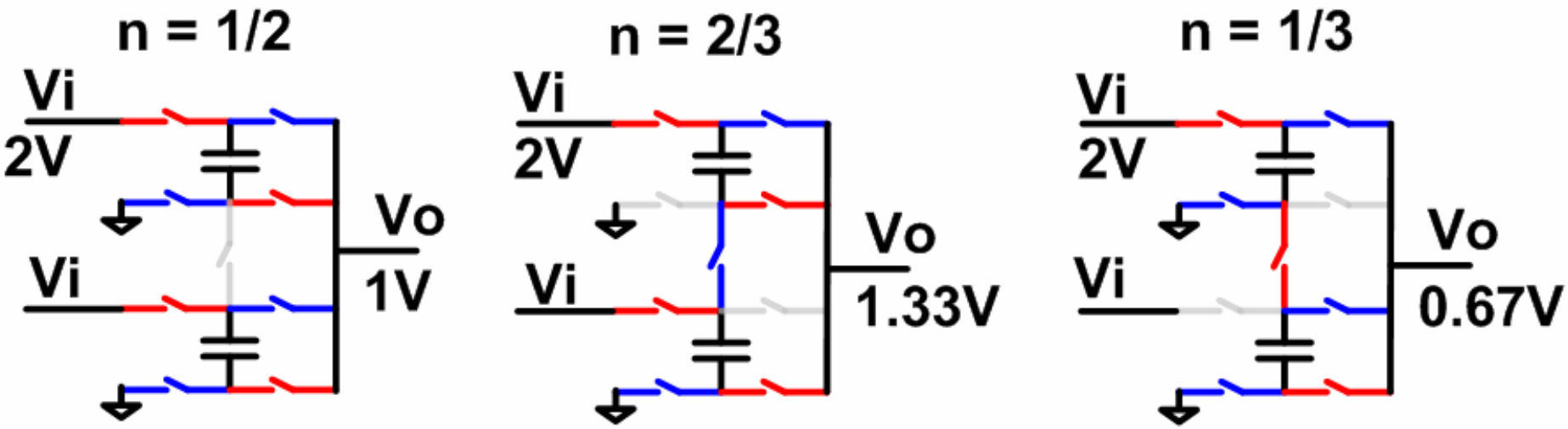
(Power ~ 1W/mm²)

Ex. 1: Integrated SC Converter Prototype



- Implemented in 32nm SOI test-chip
- Flying cap: MOS, 32-way interleaved
- Supports 0.6V ~ 1.2V from 2V input

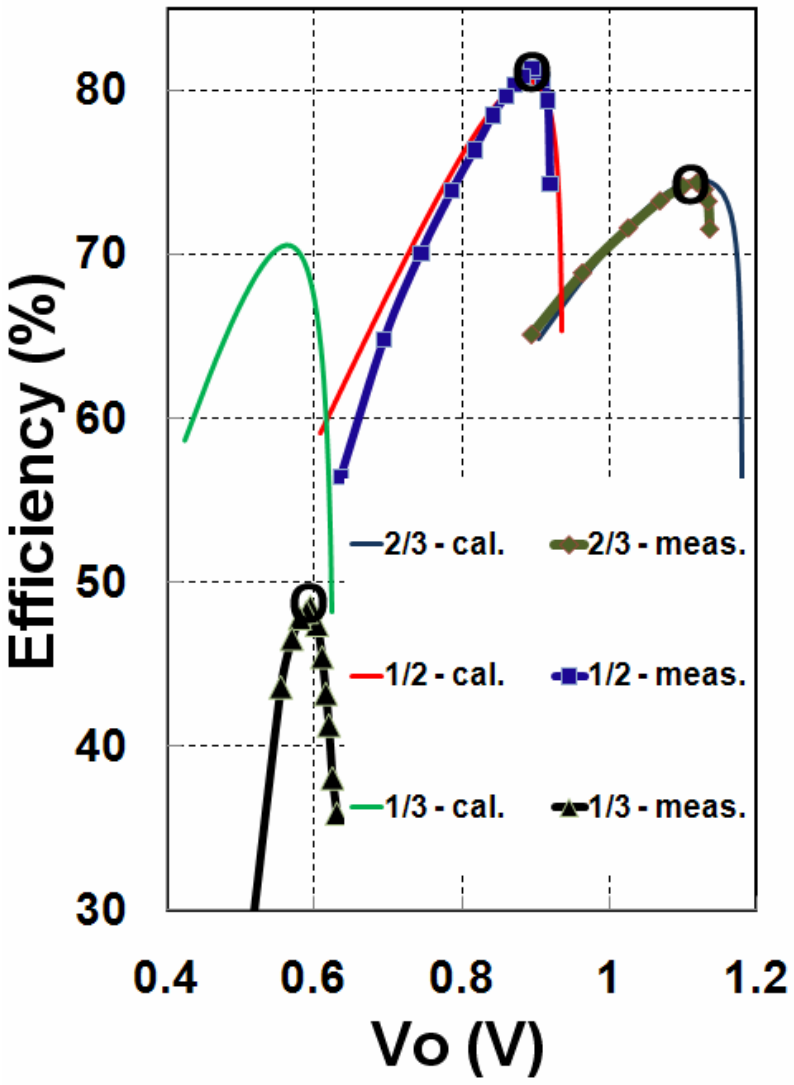
Die photo



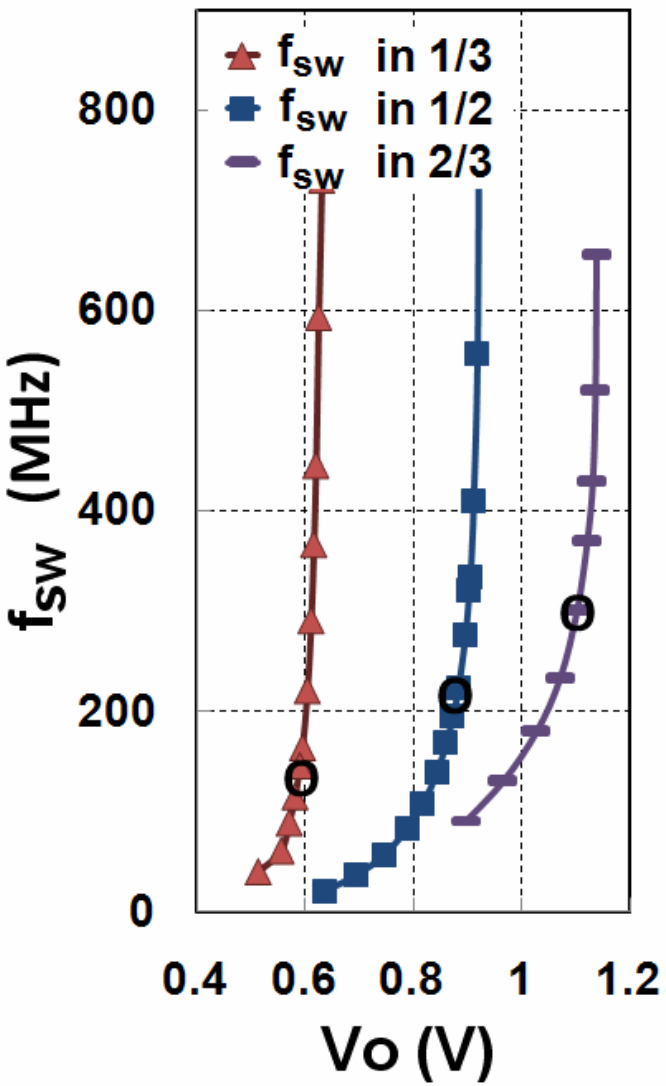
H-P Le et al, ISSCC 2010

Measured Eff. vs. Topologies

Efficiency vs. Vo



f_{sw} vs. Vo



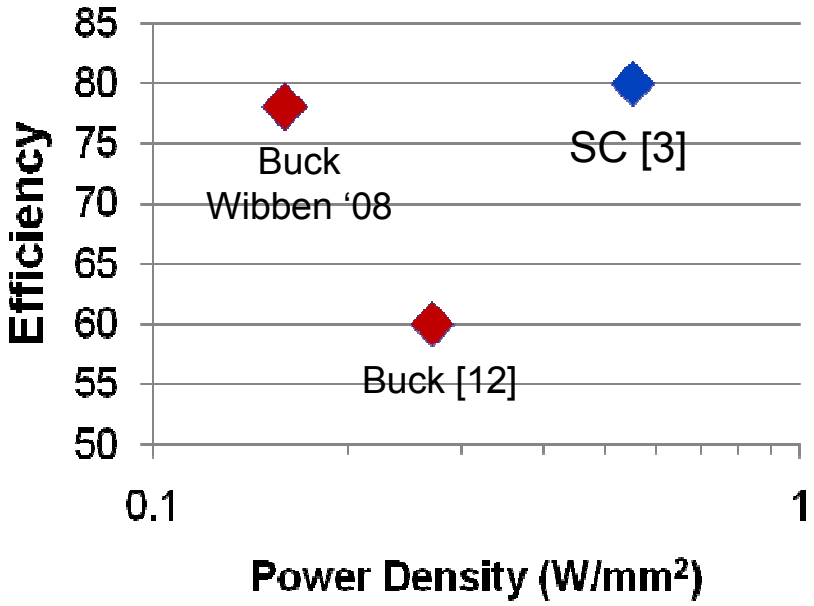
Settings:

Vi = 2V

$R_L \approx 4\Omega$ at

Vo = 0.8V

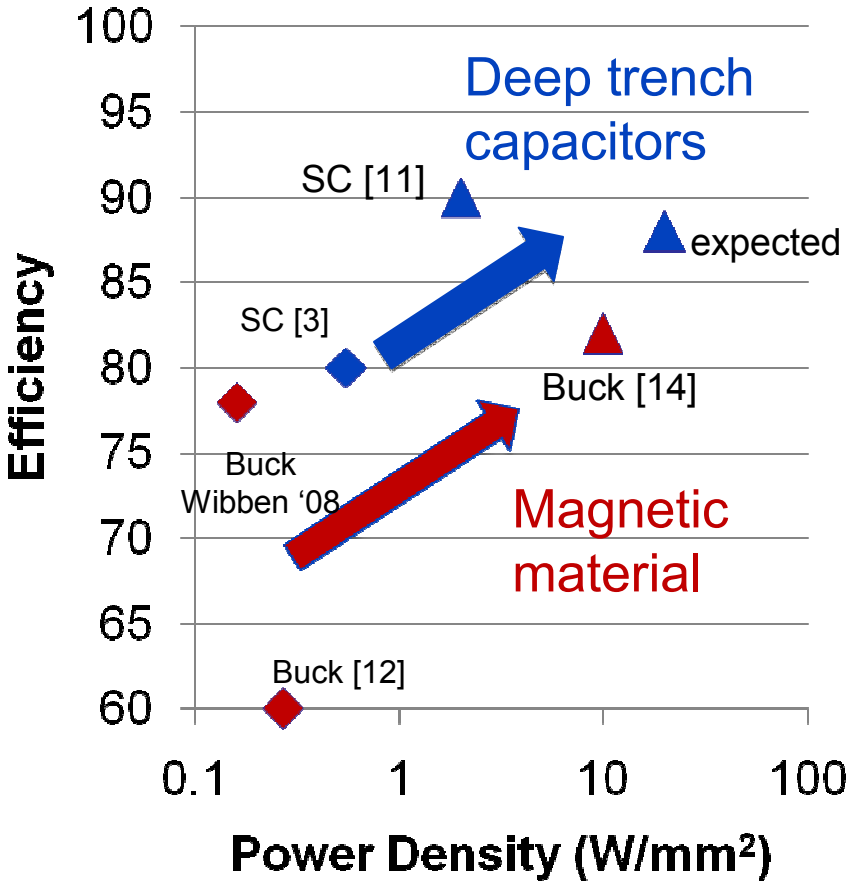
Examples with fully integrated native passives



- Capacitor constrained, ref [3] uses series-parallel
- Much higher power density and efficiency than buck
- Limited examples in plain CMOS processes

References: [3] H-P. Le, "A 32nm Fully Integrated Reconfigurable.." *ISSCC*, 2010
[12] J. Lee, "Evaluation of Fully-Integrated..." *IEEE Trans. VLSI*, 2007
J. Wibben, "A High-Efficiency DC–DC Converter…" *JSSC*, April 2008

Extra process steps allowed?

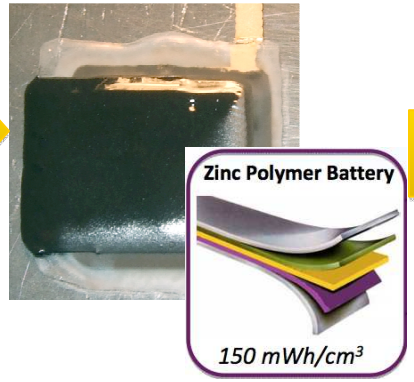


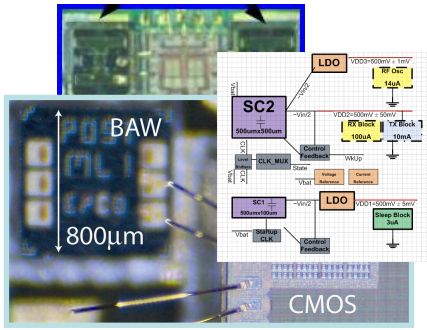
- Very high power density and efficiency expected if deep trench capacitor is used
- Deep trench capacitors are more mature than on-chip magnetic material
- SC converter can use existing decoupling cap as converter component, no extra overhead.

References: [11] L. Chang, "A fully integrated switched capacitor …" *VLSI*, 2010
[14] J. Dibene, "A 400A fully integrated silicon ..." *APEC*, 2010

Wireless Sensor Nodes & Energy Harvesting
Ex. 2: Self-Powered Active RFID Tag

- ***Self-contained*** (postage stamp footprint but only mm's thick)
- ***Fully integrated*** IC (single die)
- ***Small solar cell*** harvests enough energy for 24 hour operation





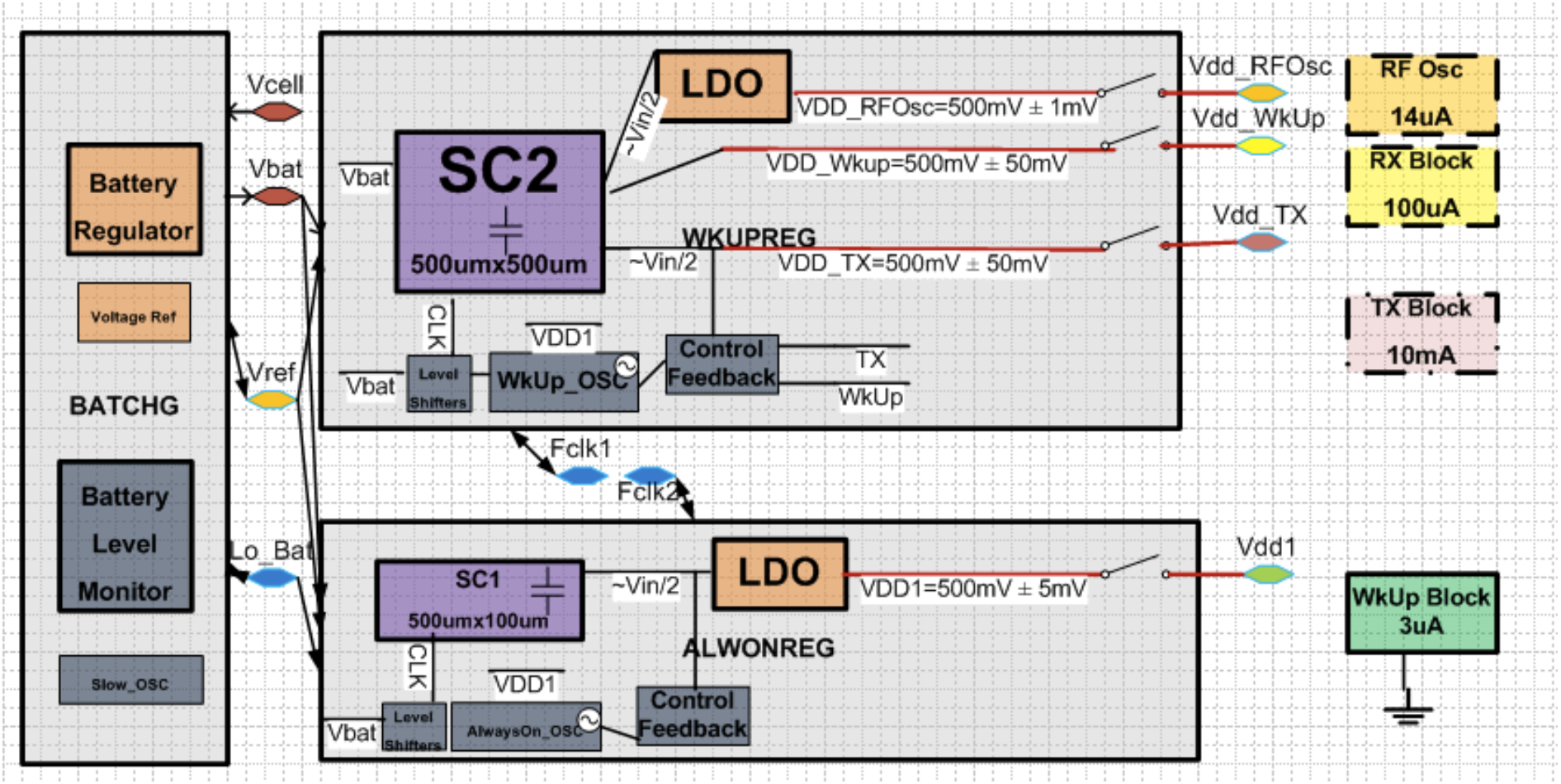
Solar Cell
- 2cmx1cm
- **10µW** avg (Indoor)
- V_{oc} = **2.4V**, I_{sc}=10uA

Printed Battery
- 1cmx1cm
- V_{bat} ~ **1.1-1.8V**
- Integration w/ substrate

Loads (on Single Die)
- 50 µW RX
- 1mW TX
- **0.5V** Logic
- On-chip power management

Berkeley Wireless Research Center

Power Subsystem Diagram



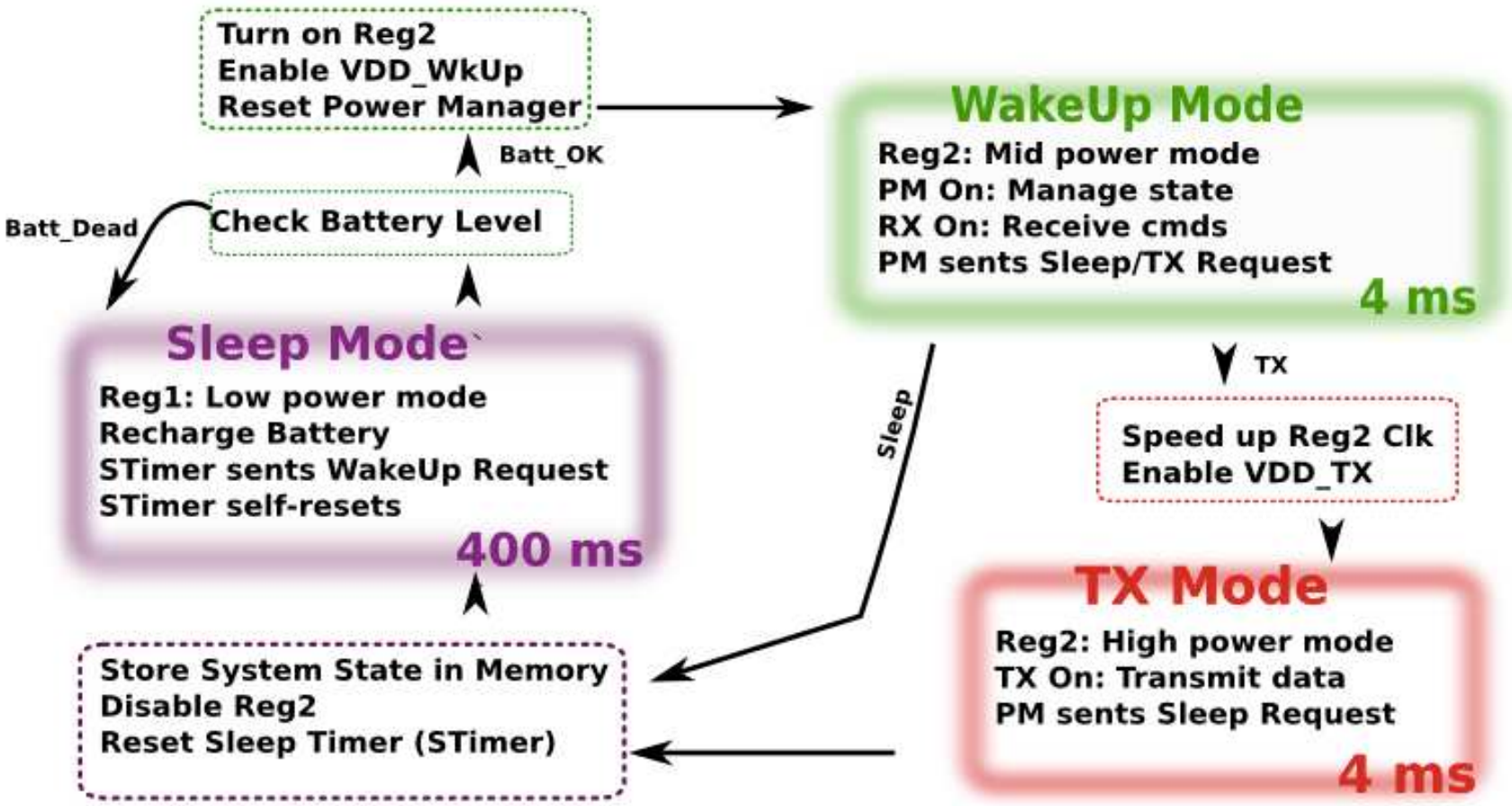
Architectures: 3:1 to 2:1 adjustable S-C's, clock speed adjusted for wake-up and again for transmit

Load Power Requirements

Rail	Clk	State (WkUp, TX)	Peak Load	Avg Load	Max Time	Ripple (mV)	Cl	Eng (uC)	Est Eff
Vdd1	100kHz	Sleep		4uA*	.4s	5mV		1.6	50% *
Vdd2_Osc	400kHz	WkUp	15.5uA	13.5uA	4ms	1mV	20fF	0.06	75%
Vdd2_RX	400kHz	WkUp	120uA	100uA	4ms	50mV	10pF	0.4	75%
Vdd2_TX	20Mhz	TX	8.5mA	7mA	10ms	50mV	20pF	~~70~~ 0.7	75%

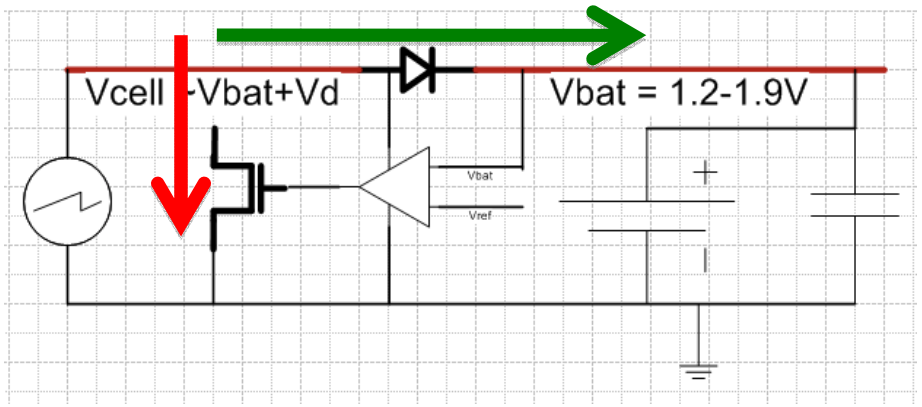
- Efficiency Estimates
  - Vdd1 assumes 90% SC, 75% LDO, 2uA Ref/Control
  - Vdd2_Osc assumes 85% SC, 90% LDO
  - Vdd2_RX assumes 85% SC, no LDO
  - Vdd2_TX assumes 80% SC, no LDO
- Clock switching frequencies are roughly the minimum for each state
  - Clks are down-converted by the controller

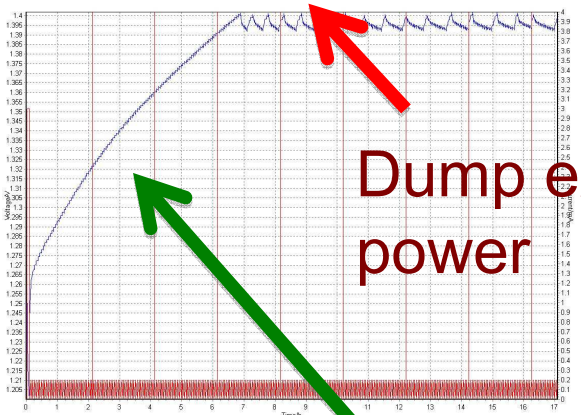
Multi-Mode Duty-Cycled Operation



Solar Cell/Battery Power Interface

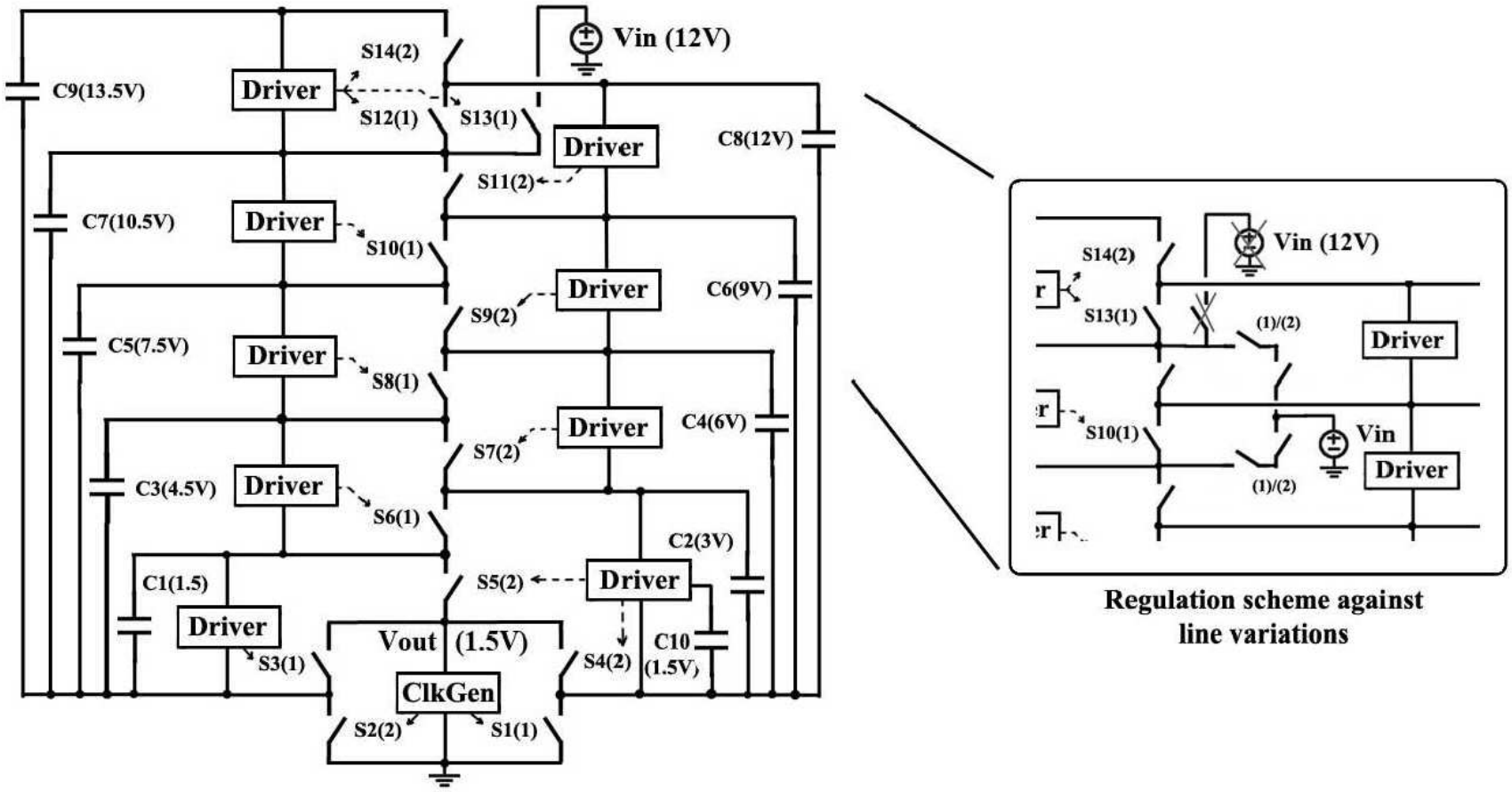
- Solar Cell/Battery Charger
  - Comparator, runs at <1Hz to minimize power
    - Set battery max threshold (e.g. 1.4V or 1.9V)
    - Signals topology choice (i.e. 2:1, 3:1)
    - Detect battery state: Dead/Low/OK/Full
  - Voltage Reference shared with regulators
  - Shunt Regulator
    - 2.5V NMOS, sized to meet max current (**250uA**) at rated Vbat (1.2-1.9V)
  - Blocking diode limits reverse leakage
    - Synchronous rectifier reduce Vd





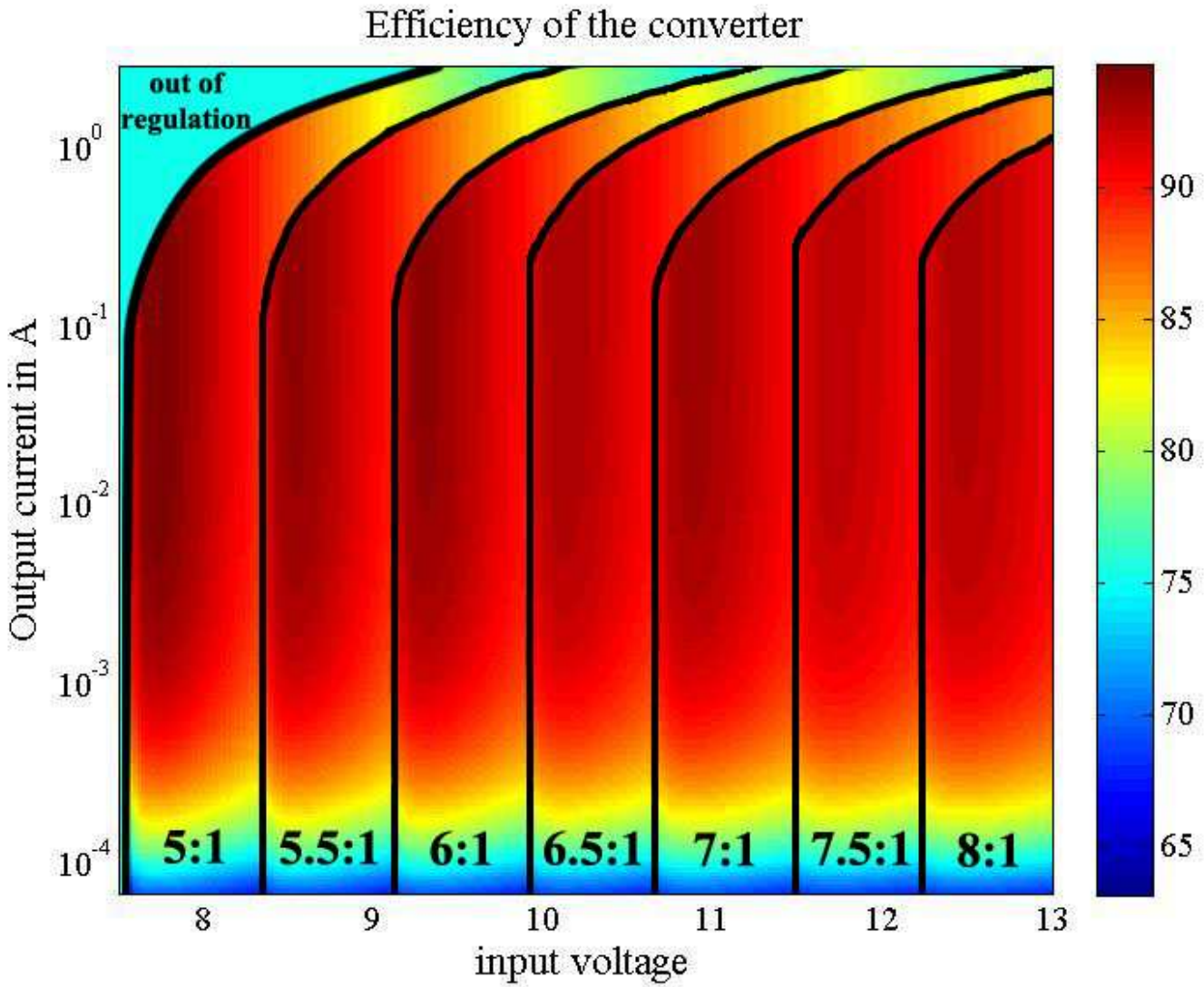
Example 3 – Point-of-Load:12V-to-1.5V Dickson Circuit

Illustrates “tap-changing” technique for line regulation.

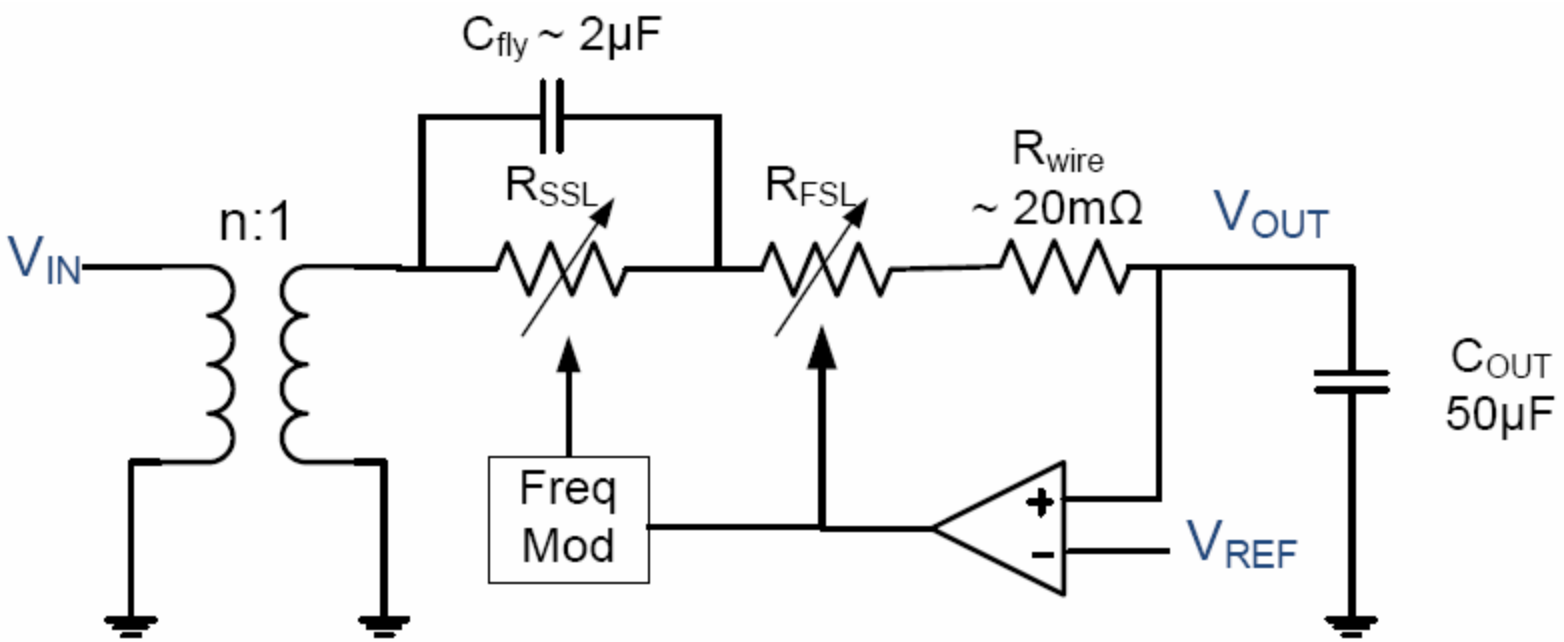


V.W. Ng, **A 98% peak efficiency 1.5A 12V-to-1.5V Switched Capacitor dc-dc converter in 0.18 um CMOS technology**, Master Thesis Report, EECS Dept, UC Berkeley, Dec. 2007, also in VLSI 2009 and ECCE 2009.

Expected efficiency over line/load

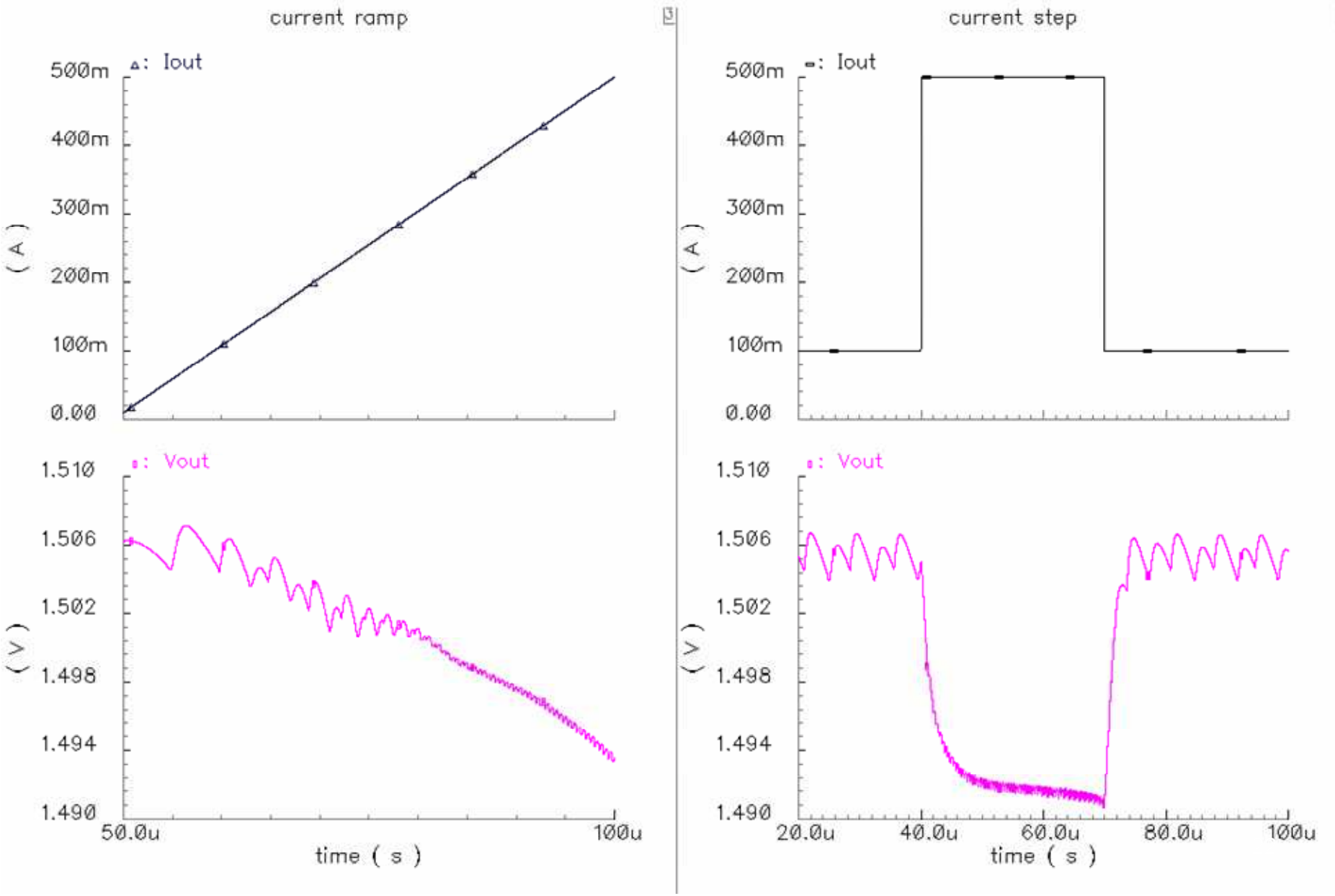


Regulation Converter model



Test IC realizing complete mode switching and fine scale regulation now in fab

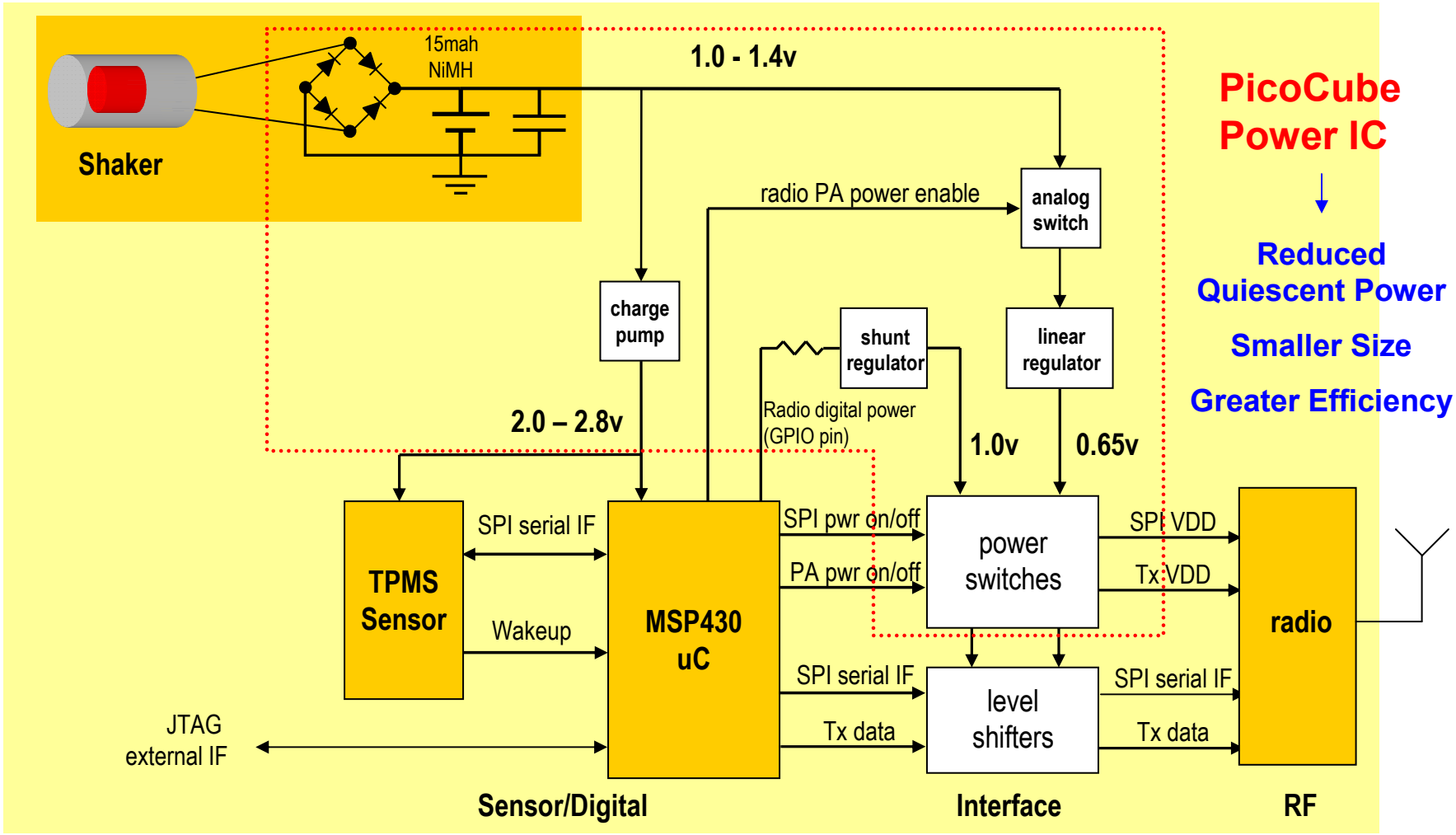
Simulation


current ramp
Iout
500m
400m
300m
200m
100m
0.00
(A)
Vout
1.510
1.506
1.502
1.498
1.494
1.490
(V)
50.0u
100u
time (s)
current step
Iout
500m
400m
300m
200m
100m
0.00
(A)
Vout
1.510
1.506
1.502
1.498
1.494
1.490
(V)
20.0u
40.0u
60.0u
80.0u
100u
time (s)

Conclusions

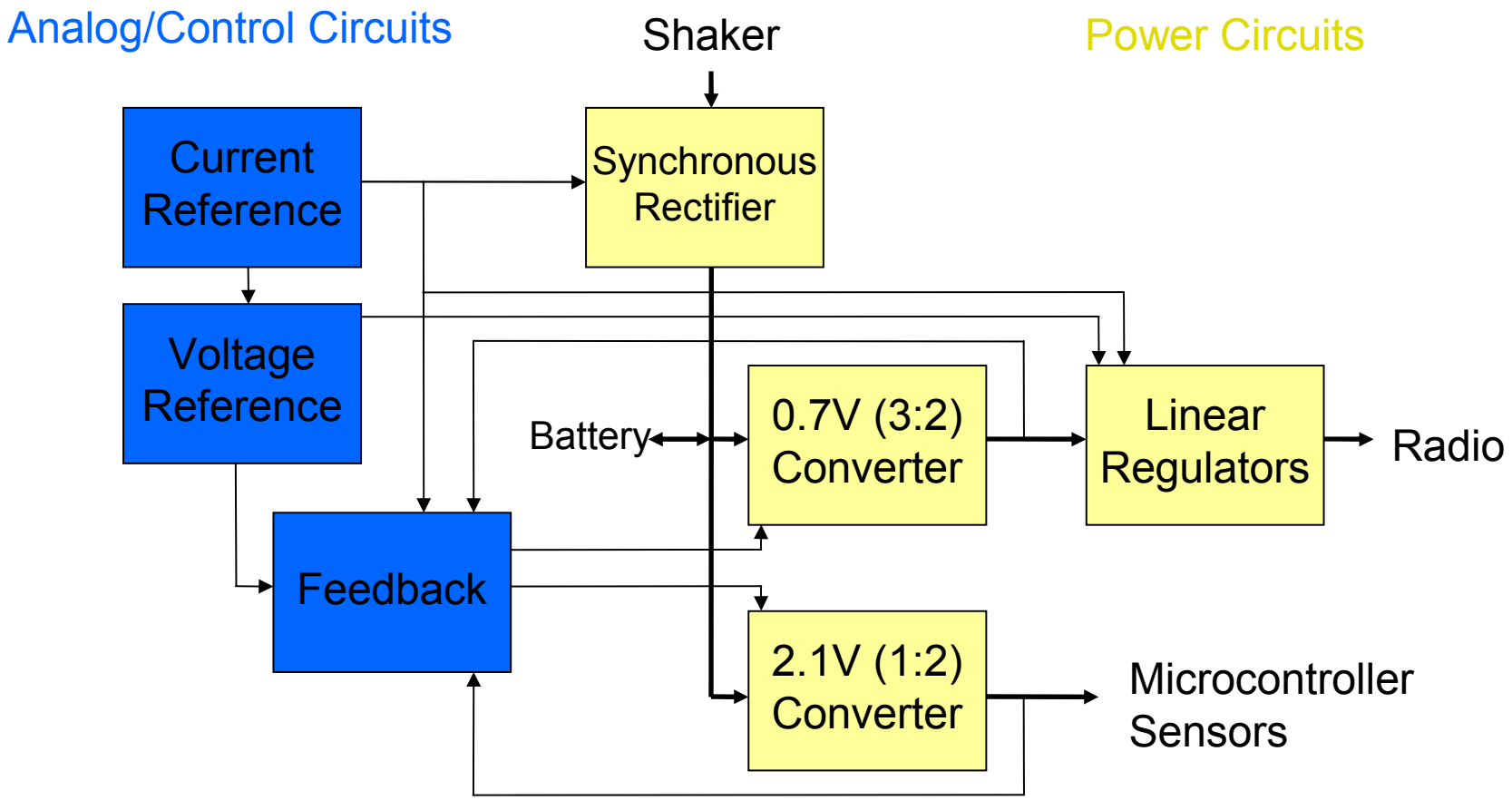
- SC converters very convenient for CMOS/ SOC integration
- Excellent utilization of switches and passive devices
- Chip and IC scale capacitors have higher useful energy and power density than inductors
- Ripple managed by extensive interleaving
- Clock scaling, on-line switch scaling, and drive amplitude techniques convenient for low and ultra-low power operation
- Regulation potential challenge

Ex. 3 - Ultra-low-power Conversion in PicoCube Wireless Sensor Node



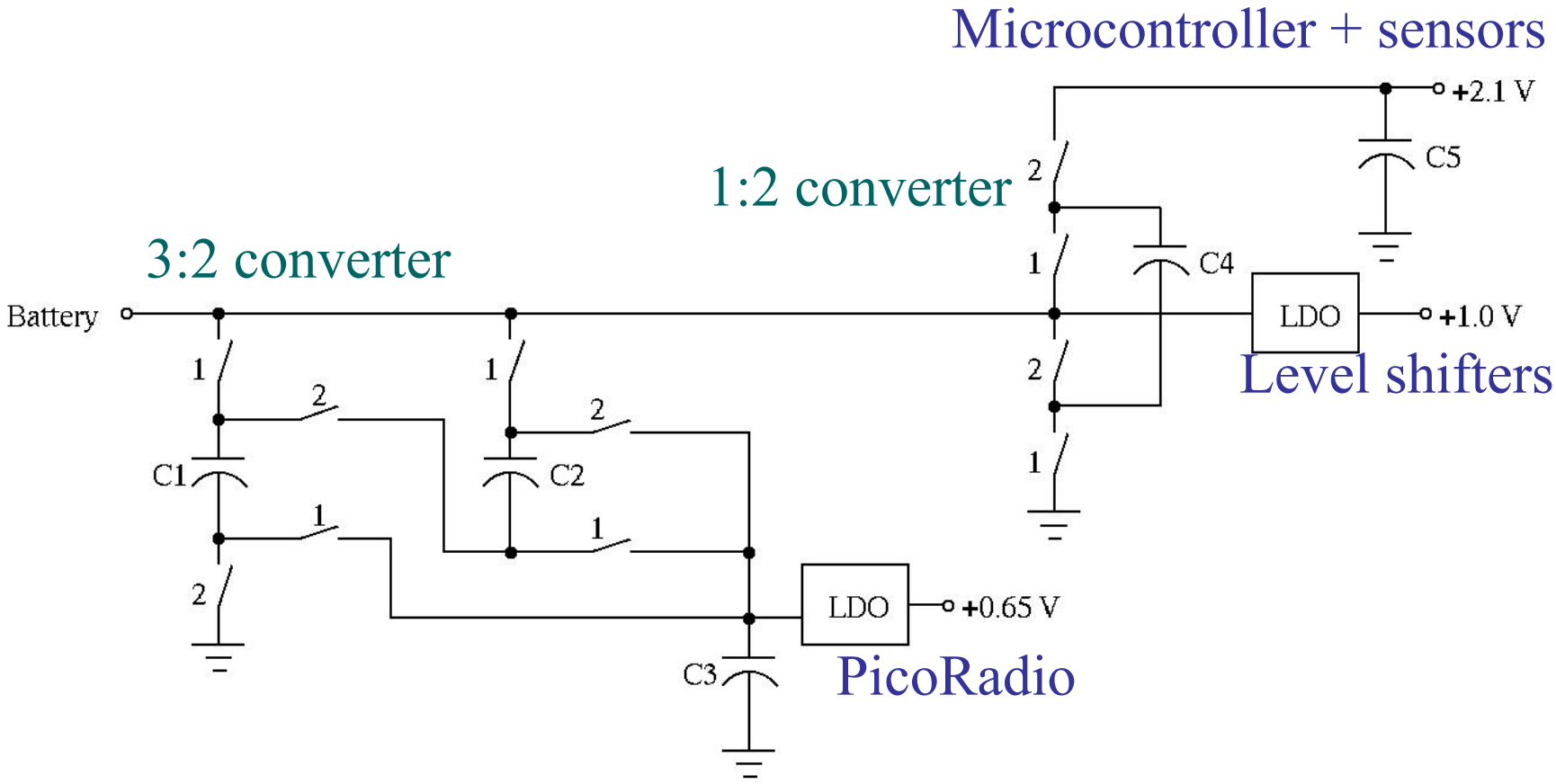
PicoCube: A 1cm3 Sensor Node Powered by Harvested Energy, 2008 DAC/ISSCC Student Design Contest

PicoCube Power Management Chip Block Diagram



Seeman, Sanders, Rabaey, "An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes," *CICC* 2007.

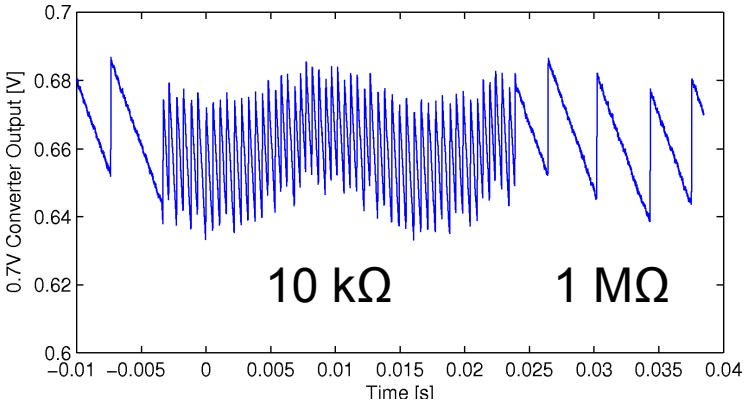
PicoCube Converter Topology

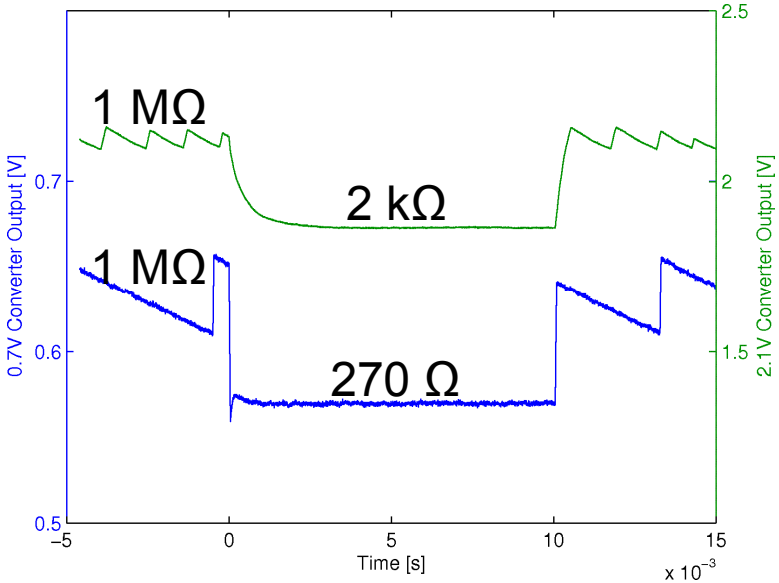


Linear Regulators (LDOs) further regulate and reduce ripple on outputs

Hysteretic Feedback

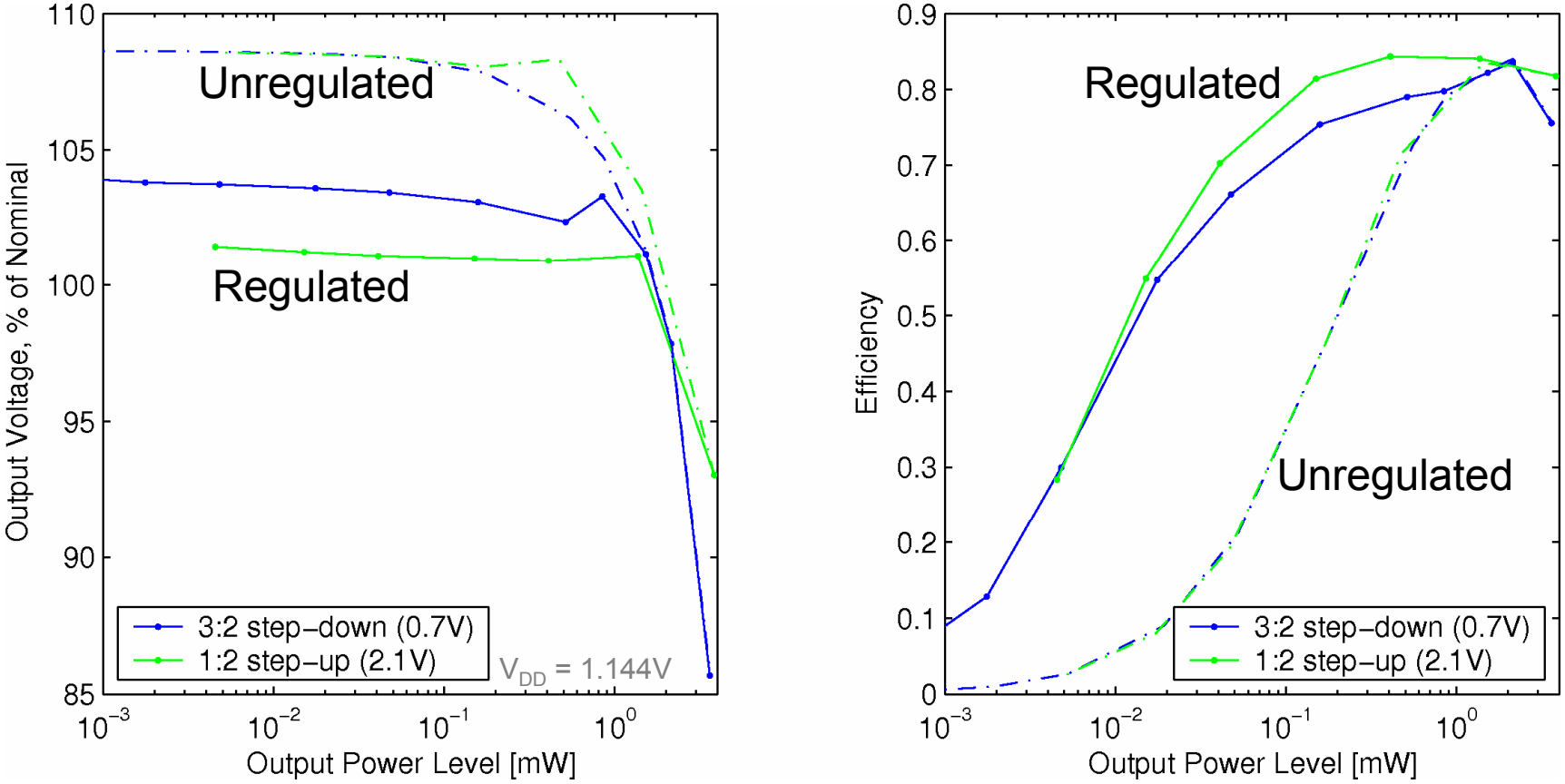
- Regulates output voltage
  - On/off clocking control
  - Thermostat-type control
  - Improves efficiency by reducing f_{sw} for small loads





Converter leaves regulation for only large loads

Converter Performance

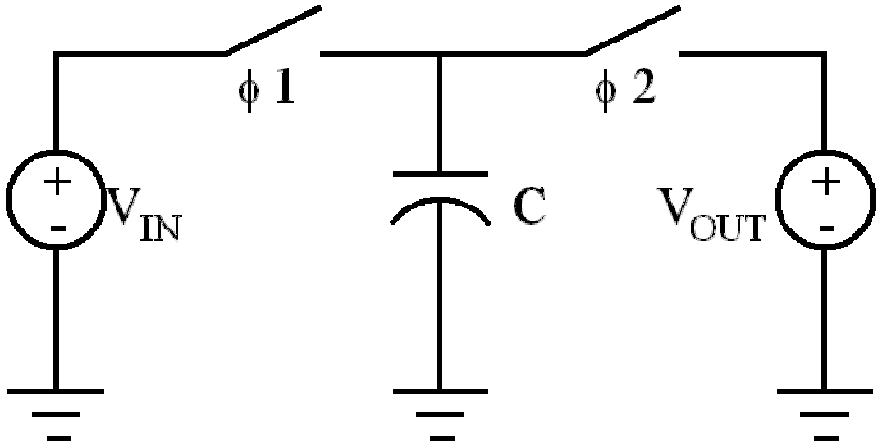


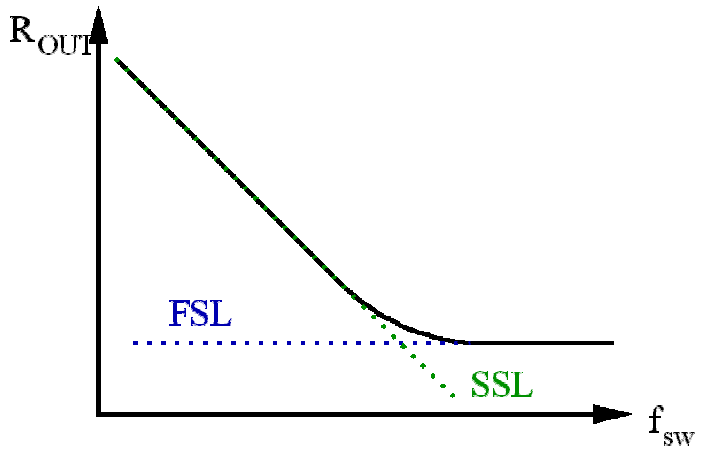
Regulation is effective at controlling output voltage and increasing efficiency at low power levels!

Why Not S-C ?

- Difficult regulation?
- Not suited for high current/power? X
- Interconnect difficulty for many caps? X
- Voltage rating of CMOS processes? X
- Magnetic-based ckts = higher performance? X
- Ripple? X

SC Analysis: Simplest Example





- Slow Switching Limit (SSL):
  - Impulsive currents (charge transfers)
  - Resistance negligible (assume R = 0)
  - This (SSL) impedance is the switching loss!
- Fast Switching Limit (FSL):
  - Constant current through switches
  - Model capacitors as voltage sources (C → ∞)

$$i = f_{sw}\Delta q = \boxed{f_{sw}C\Delta v}$$

$$i = \boxed{\frac{1}{4}\frac{1}{R}}\Delta v$$

$$(\Delta v = V_{IN} - V_{OUT})$$

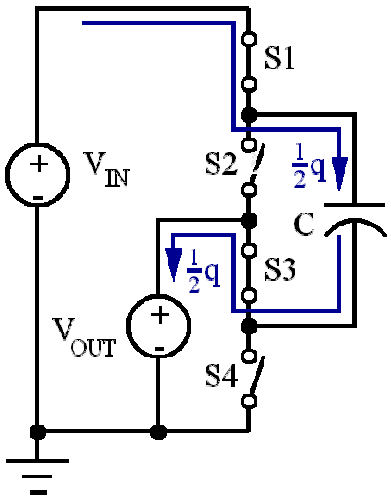
Analysis via Charge Multipliers

Capacitor Charge Multiplier:

$$a_{c,i}^{j} = \frac{\text{charge flow in cap } i\text{, phase } j}{\text{output charge flow, both phases}}$$

Switch Charge Multiplier:

$$a_{r,i} = \frac{\text{charge flow in switch } i\text{, when on}}{\text{output charge flow, both phases}}$$

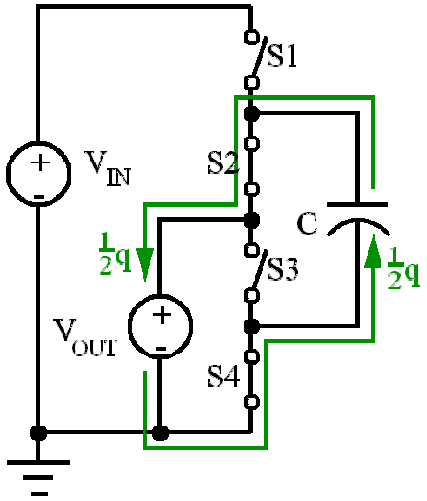


Phase 1:

$a_c^1 = \frac{1}{2}$

$a_{r,1} = \frac{1}{2}$

$a_{r,3} = -\frac{1}{2}$



Phase 2:

$a_c^2 = -\frac{1}{2}$

$a_{r,2} = \frac{1}{2}$

$a_{r,4} = -\frac{1}{2}$

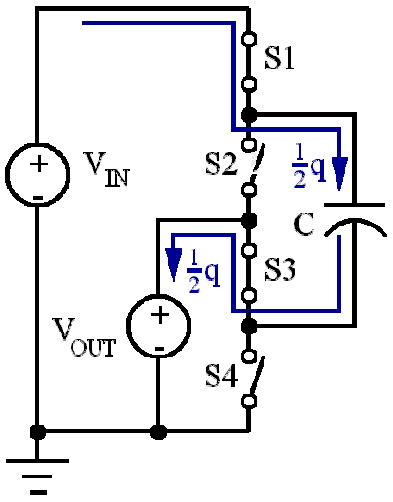
Analysis via Charge Multipliers

Capacitor Charge Multiplier:

$$a_{c,i}^{j} = \frac{\text{charge flow in cap } i\text{, phase } j}{\text{output charge flow, both phases}}$$

Switch Charge Multiplier:

$$a_{r,i} = \frac{\text{charge flow in switch } i\text{, when on}}{\text{output charge flow, both phases}}$$

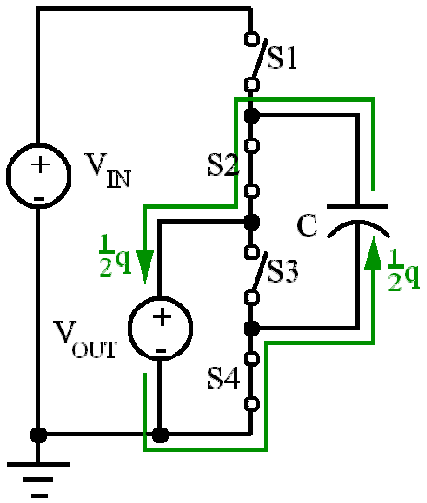


Phase 1:

$$a_c^1 = \tfrac{1}{2}$$

$$a_{r,1} = \tfrac{1}{2}$$

$$a_{r,3} = -\tfrac{1}{2}$$



Phase 2:

$$a_c^2 = -\tfrac{1}{2}$$

$$a_{r,2} = \tfrac{1}{2}$$

$$a_{r,4} = -\tfrac{1}{2}$$

Output Impedance ~ Power Loss

M. Seeman, S. Sanders, IEEE T-PELS, March 2008

- An SC converter's power loss is the sum of component energy (power) losses:

$$P_{SSL} = f_{sw} \sum_{capacitors} \Delta q_i \Delta v_i = R_{SSL} i_{OUT}^2 \qquad P_{FSL} = \frac{1}{2} \sum_{switches} R_i \left(2 q_i f_{sw}\right)^2$$

- The converter's output impedance can be determined in terms of just the charge multiplier components:

$$R_{SSL} = \sum_{capacitors} \frac{(a_{c,i})^2}{C_i f_{sw}} \qquad R_{FSL} = 2 \sum_{switches} R_i (a_{r,i})^2$$

Output Impedance and Optimization

Tellegen's theorem and energy conservation used to find R_{OUT}:

SSL: $$R_{OUT} = \frac{1}{f_{sw}} \sum_{i \in capacitors} \frac{(a_{c,i}^1)^2}{C_i}$$

FSL: $$R_{OUT} = 2 \sum_{i \in switches} R_i (a_{r,i})^2$$

Minimize output impedance while keeping component cost constant:

Cost constraint	**Optimized components**	**Optimized output impedance**
$E_{TOT} = \frac{1}{2} \sum_{capacitors} C_i v_{c,i(rated)}^2$	$\Longrightarrow \quad C_i^* \propto \left\| \frac{a_{c,i}}{v_{c,i(rated)}} \right\|$	$R_{SSL}^* = \frac{1}{2E_{TOT} f_{sw}} \left(\sum_{capacitors} \left\| a_{c,i} v_{c,i(rated)} \right\| \right)^2$
$A_{TOT} = \sum_{switches} G_i v_{r,i(rated)}^2$	$\Longrightarrow \quad G_i^* \propto \left\| \frac{a_{r,i}}{v_{r,i(rated)}} \right\|$	$R_{FSL}^* = \frac{2}{A_{TOT}} \left(\sum_{switches} \left\| a_{r,i} v_{r,i(rated)} \right\| \right)^2$

In the optimal case:

- Capacitor voltage ripple and switch voltage drop are proportional to rated voltage
- Output impedance proportional to the square of the *sum of the component V-A produ*

Comparing Converters

Need a metric to compare converters of different types!

Example: How much power can we get out of a converter with 10% voltage drop?

$$P_{OUT} = I_{OUT} V_{OUT} = (0.1 G_{OUT} V_{OUT}) V_{OUT} = 0.1 \cdot G_{OUT} V_{OUT}^2$$

Power performance related to GV^2

We can make a unitless performance metric by comparing converter GV^2 to component GV^2

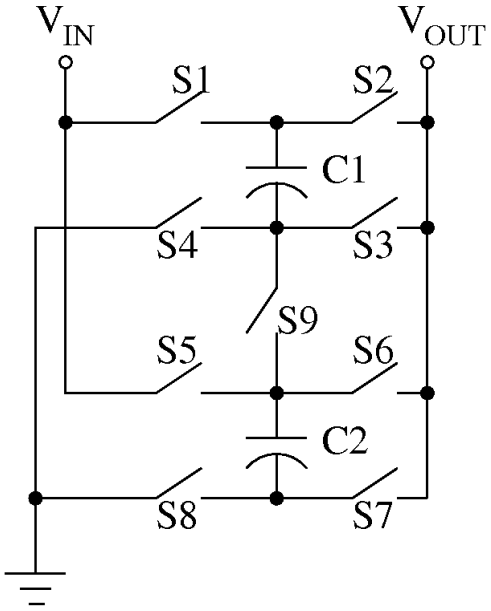
"Slow-Switching Limit" (SSL) Metric:

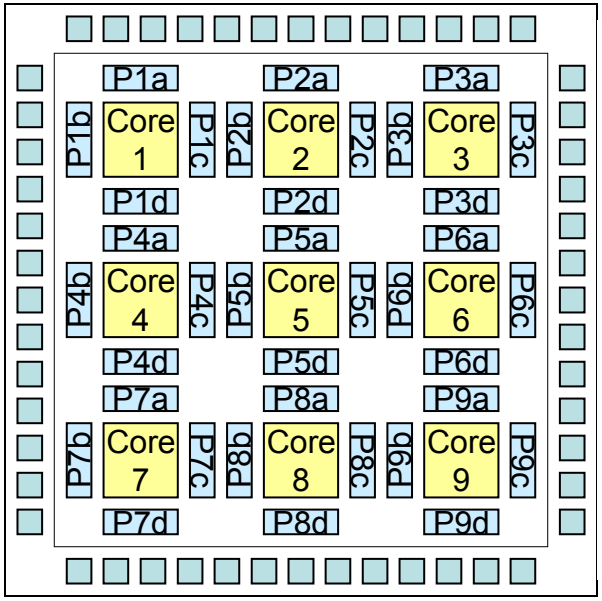
$$\frac{G_{OUT} V_{OUT}^2}{f \sum_{caps} C_i v_{c,i(rated)}^2}$$

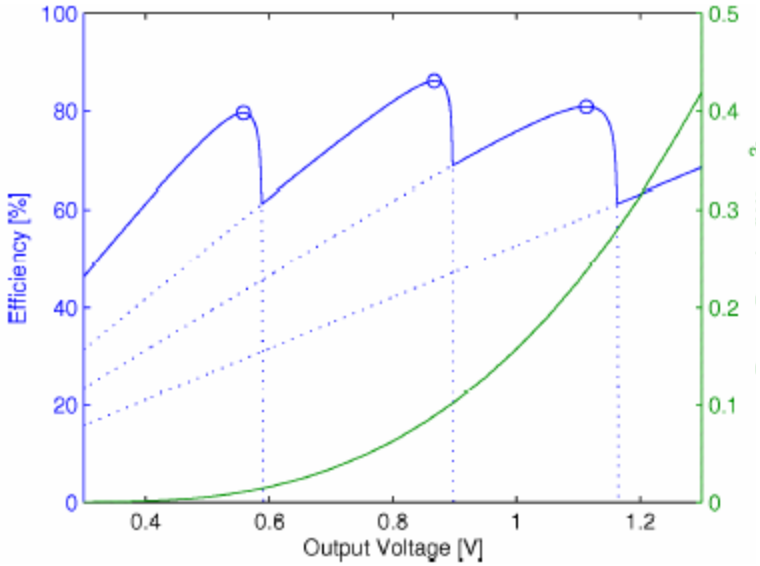
"Fast-Switching Limit" (FSL) Metric:

$$\frac{G_{OUT} V_{OUT}^2}{\sum_{switches} G_i v_{r,i(rated)}^2}$$

Ex. 3: Microprocessor SC Converter



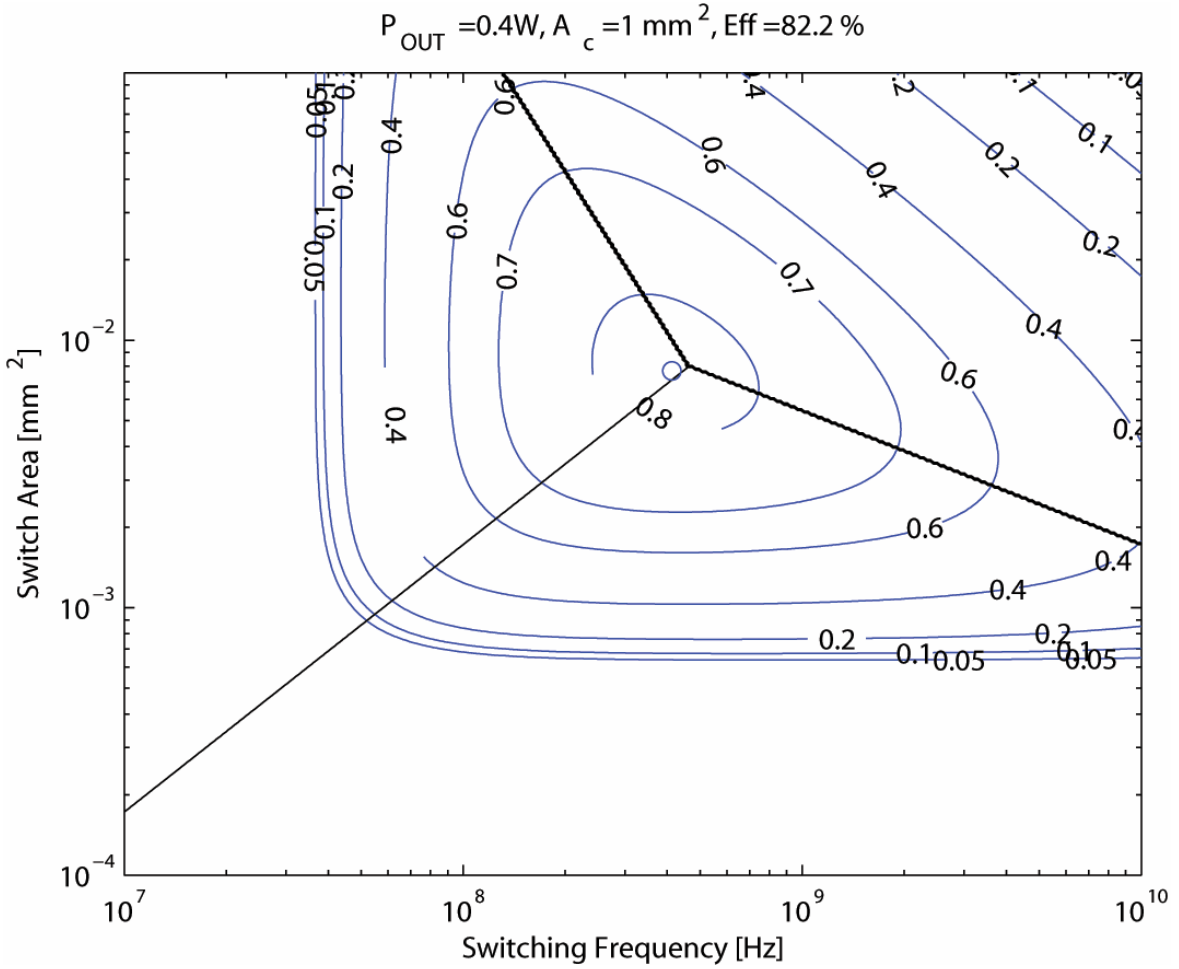




- A power density of 1 W/mm^2 is achievable in 65nm process.
- A tiled design improves output ripple and ESR performance
- Creates a scalable IP platform
- Ideal for microprocessor supplies:
  - Ultra-fast transient response
  - Package I/O at higher voltage/lower current
  - Independent core voltage control

Design Optimization Example: 0.4 W/sq.mm

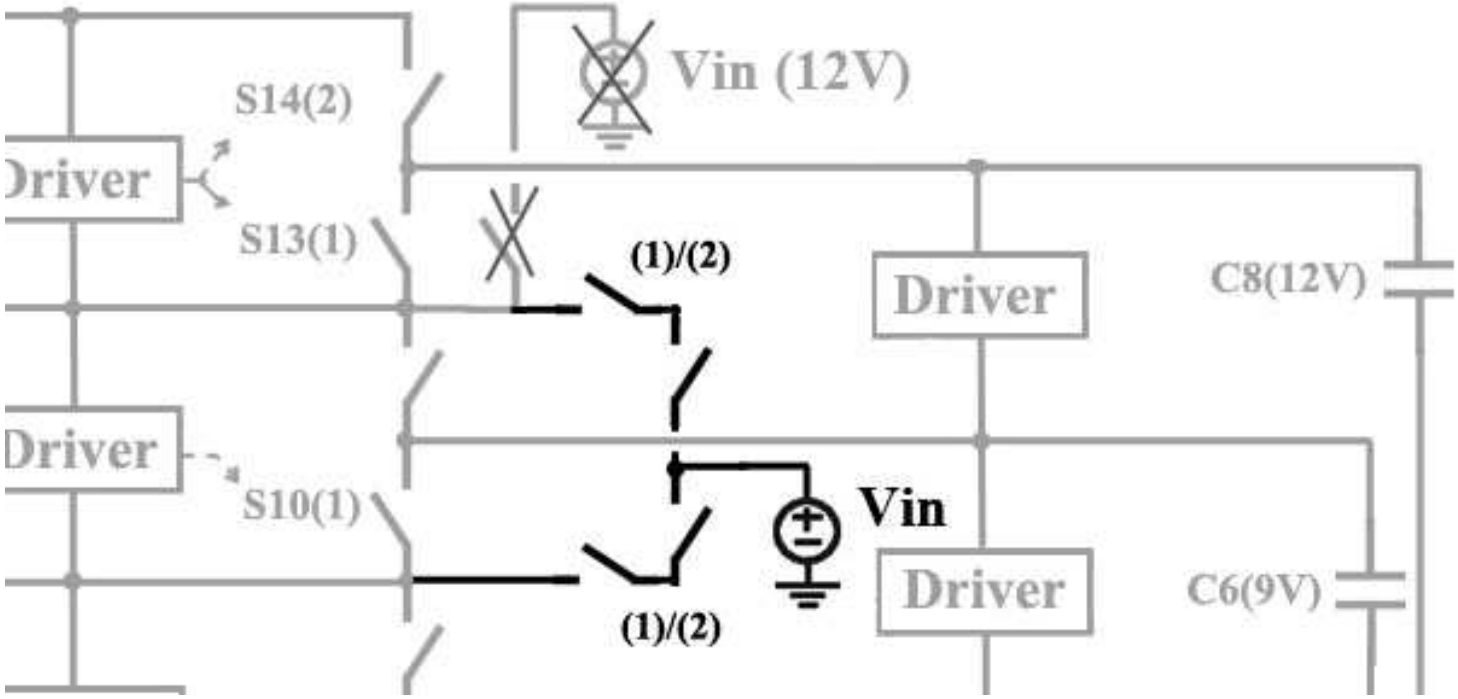
- Representative 0.13um tech
- 2.4-to-1.2V Conversion
- 1 sq mm M-I-M cap (2 nF)
- Losses
  - SSL (main caps)
  - FSL (conduction)
  - Gate cap
  - Cap Bottom plate
  - Junction cap



Switched Cap Take-Aways

- Theoretical performance exceeds magnetic-based converters, and this is being realized in research
- Very simple low power operation – reduce clk
- Integration convenient for v. low power app's to v. high current app's
- Moderate (high) voltage capability by stacking devices – triple-well, SOI
- Regulation challenges – nominal fixed ratio, but can operate with multiple Taps
- Further on-chip integration via aggressive clk scaling

- Tap Changing for Line Regulation – Feedforward



- Multi-mode Operation for Apps like Voltage Scaling

Output Impedance ~ Power Loss

M. Seeman, S. Sanders, IEEE T-PELS, March 2008

- An SC converter's power loss is the sum of component energy (power) losses:

$$P_{SSL} = f_{sw} \sum_{capacitors} \Delta q_i \Delta v_i = R_{SSL} i_{OUT}^2 \qquad P_{FSL} = \frac{1}{2} \sum_{switches} R_i \left(2 q_i f_{sw}\right)^2$$

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Output Impedance and Optimization

Tellegen's theorem and energy conservation used to find R_{OUT}:

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$A_{TOT} = \sum_{switches} G_i v_{r,i(rated)}^2$	$\Longrightarrow \quad G_i^* \propto \left\| \frac{a_{r,i}}{v_{r,i(rated)}} \right\|$	$R_{FSL}^* = \frac{2}{A_{TOT}} \left(\sum_{switches} \left\| a_{r,i} v_{r,i(rated)} \right\| \right)^2$

In the optimal case:

- Capacitor voltage ripple and switch voltage drop are proportional to rated voltage
- Output impedance proportional to the square of the *sum of the component V-A produ*

D.H. Wolaver, PhD dissertation,MIT,1969 proves fundamental thms on dc-dc conv.:

G = voltage or current gain

- Switches (*resistors*):

$$-\sum_{k\in dc-active}\bar{v}_k\bar{i}_k \geq \frac{G-1}{G}P_O \qquad -\sum_{k\in ac-active}\overline{(v_k-\bar{v}_k)\bullet(i_k-\bar{i}_k)}\geq \frac{G-1}{G}P_O$$

- *Ladder/Dickson are optimal*

- Reactive Elements:

$$\frac{1}{2}\sum_{k\in reactive}\left|\overline{v_k i_k}\right| \geq \frac{G-1}{G}P_O$$

Meaning for 2-phase ckts:

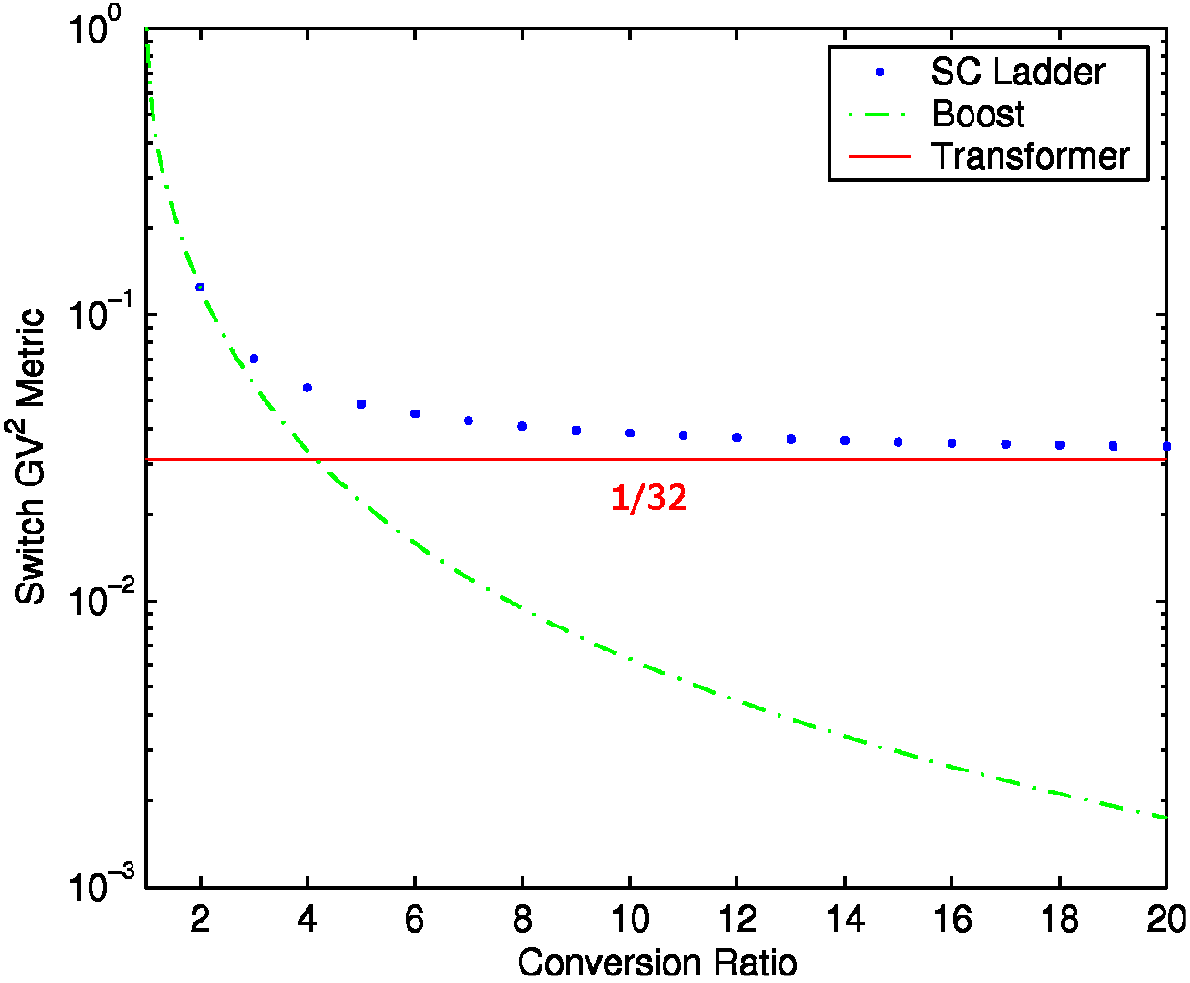
$$\sum_{k\in C}V_k q_k + \sum_{k\in L}I_k\lambda_k \geq \frac{1}{f}\frac{G-1}{G}P_O$$

Conduction Loss Comparison

M. Seeman, S. Sanders, IEEE T-PELS, March 2008

•Performance compared with switch GV² metric:

$$\frac{G_{OUT}V_{OUT}^2}{\sum G_i v_{r,i(rated)}^2}$$



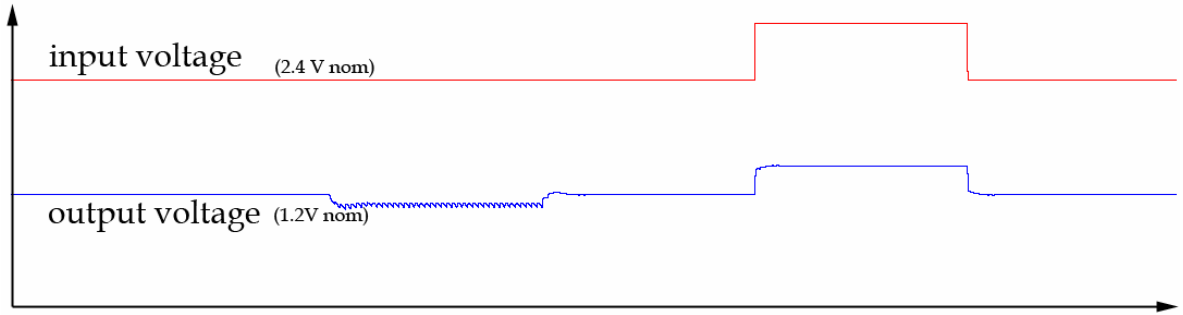
•Since converters are bi-directional, graph applies equally to step-down converters

•Magnetic components modeled with *zero* conduction loss, and *no* switching loss impact

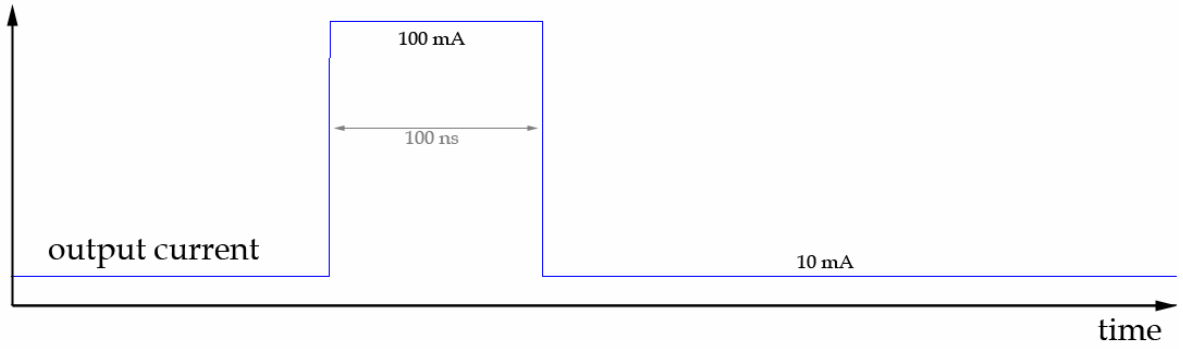
Regulation Considerations

- *Open-Loop* Loadline Regulation
  - Droop matching resistive output impedance effective for loadline VR type reg.

Dominant First Order Dynamics



Simulation Example: 8-phase 2-to-1 converter



- Tap Changing for Line Regulation – Feedforward
- Multi-mode Operation for Apps like Voltage Scaling

Comparative Energy Densities of Representative SMT Components

Type	Manufacturer	Capacitance	Dimensions WxLxH [mm³]	Energy Density [μJ/mm³]
Ceramic	Taiyo-Yuden	22 μF @ 4V	1.6x0.8x0.8 (0603)	344
	Taiyo-Yuden	1 μF @ 35V	1.6x0.8x0.8 (0603)	1196
Tantalum	Vishay	10 μF @ 4V	1.0x0.5x0.6	533
	Vishay	100 μF @ 6.3V	2.4x1.45x1.1	1037
Electrolytic	Kemet	100 μF @ 6.3V	7.3x4.3x2.8	45
	Kemet	22 μF @ 16V	7.3x4.3x1.9	94
	C.D.E.	210 mF @ 50V	76ϕx219	172

(a)

Type	Manufacturer	Inductance	Dimensions WxLxH [mm³]	Energy Density [μJ/mm³]
Shielded SMT	Coilcraft	10 μH @ 0.21 A	2.6x2.1x1.8	0.045
Shielded SMT	Coilcraft	100 μH @ 0.10 A	3.4x3.0x2.0	0.049
Shielded	Coilcraft	170 μH @ 1.0A	11x11x9.5	0.148
Shielded	Murata	1 mH @ 2.4A	29.8ϕx21.8	0.189

(b)

>1000:1 greater energy density ratio (cap:ind), in small discretes

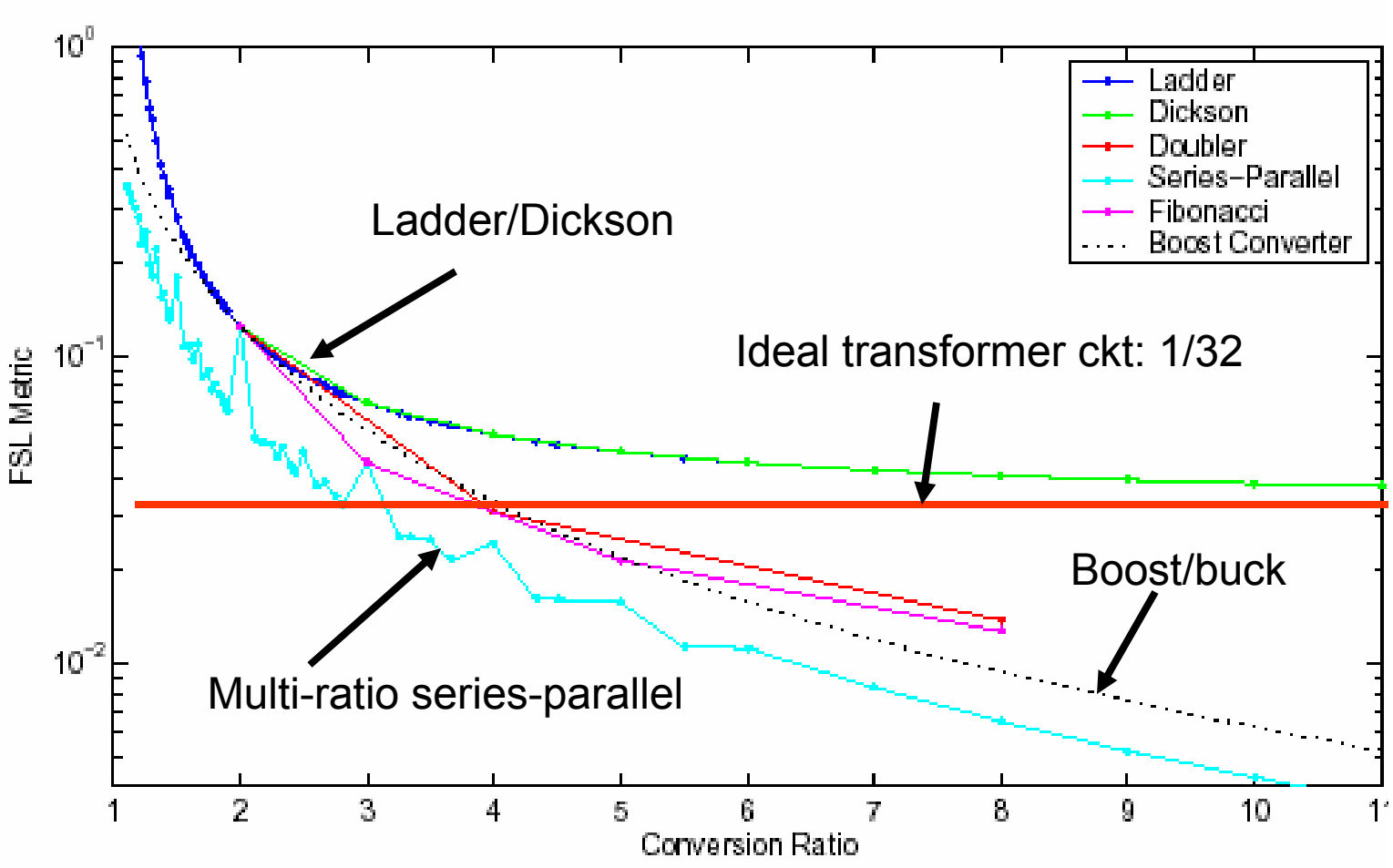
M. Seeman, PhD Dissertation, EECS Dept, UC Berkeley, 2009

Switch Utilization – Conduction Loss Comparison

- Performance compared with switch GV2 metric:

$$\frac{G_{OUT}V_{OUT}^2}{\sum G_i v_{r,i(rated)}^2}$$

- Magnetic components modeled with *zero* conduction loss, and *no* switching loss impact



Reactive Component Comparison:

D.H. Wolaver, PhD dissertation,MIT,1969: fundamental thms on dc-dc conv.:

G = voltage or current gain

"Time avg of absolute value of V-A prod."

$$\frac{1}{2}\sum_{k\in reactive}\overline{|v_k i_k|} \geq \frac{G-1}{G} P_O$$

Meaning for standard 2-phase ckts:

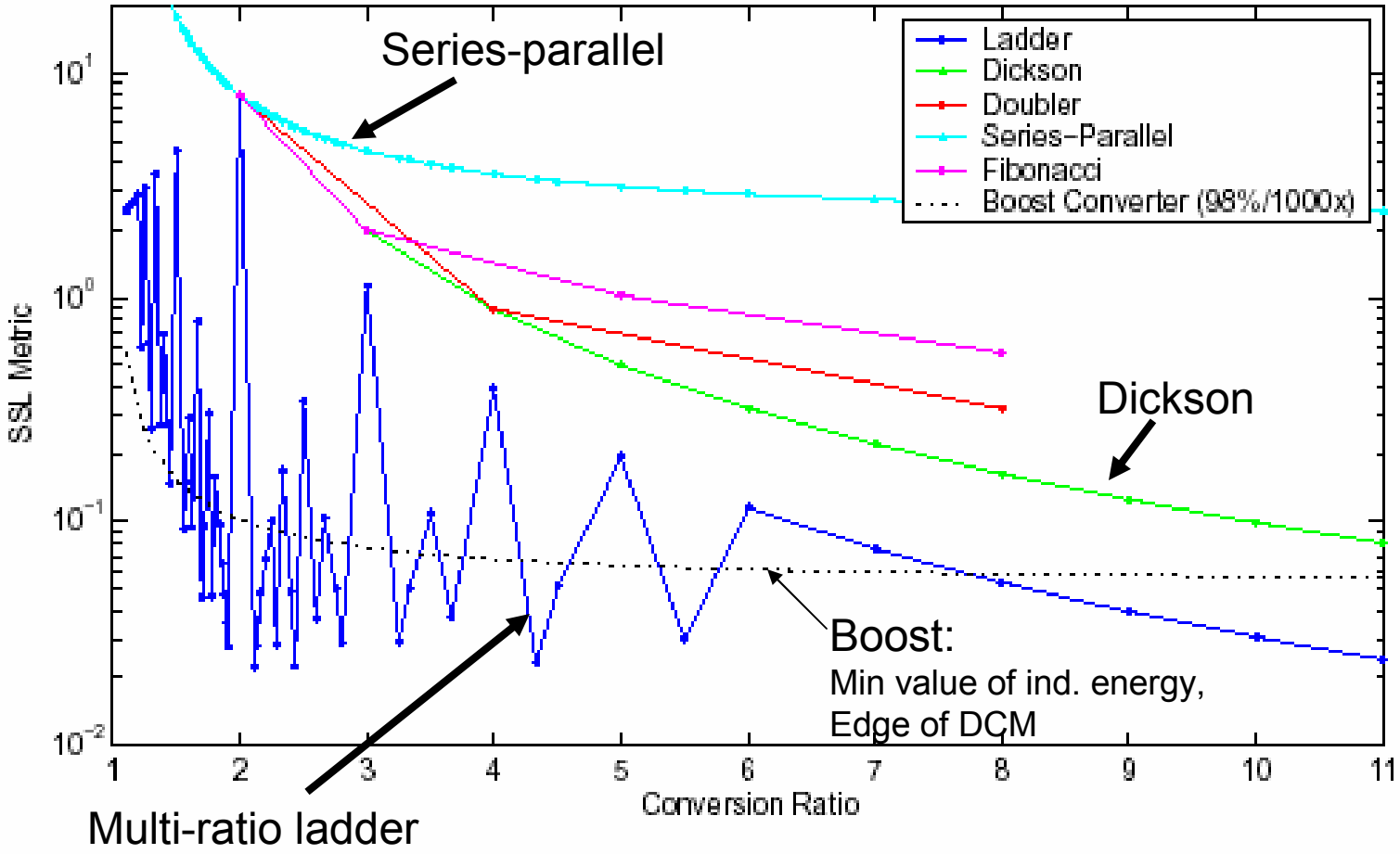
$$\sum_{k\in C} V_k \Delta q_k + \sum_{k\in L} I_k \Delta \lambda_k \geq \frac{1}{f}\frac{G-1}{G} P_O$$

Vdc-deltaQ Idc-deltaFlux

Utilization of Reactive Elements:

SC: $0.02 \bullet \dfrac{G_{OUT} V_{OUT}^2}{f \sum_{caps} C_i v_{c,i(rated)}^2}$ Versus Mag: $0.001 \bullet \dfrac{P_{OUT}}{f \bullet \frac{1}{2} L I^2}$

$$\frac{G_{OUT} V_{OUT}^2}{f \sum_{caps} C_i v_{c,i(rated)}^2}$$



The Submicron Opportunity

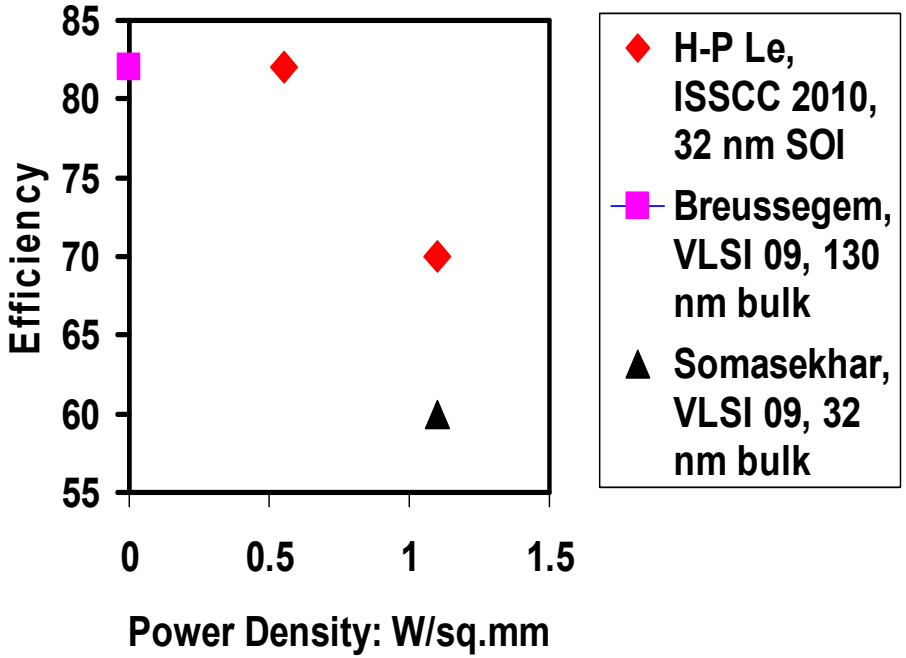
- Rate device by ratio: $G_s V_s^2 \big/ C V_g^2$
  - Essentially an Ft type parameter for a power switch reflecting power gain, exposes opportunity in scaling
- Suggests that we should look for opportunities to build our ckts with scaled CMOS based devices, but:
  - Low voltage rating per device
  - Inadequate metal/interconnect for high current?

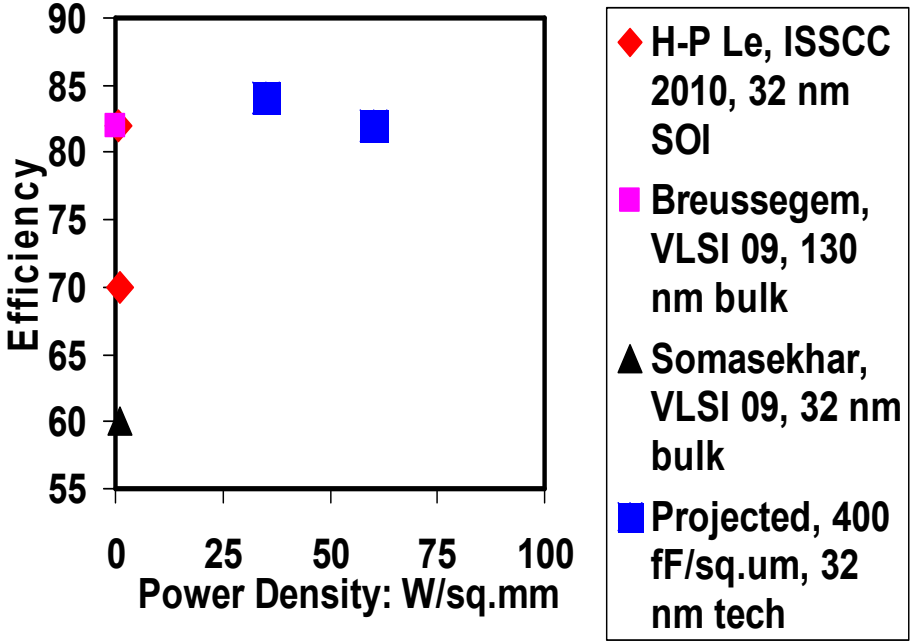
Comparison with Other Work

Work	[1]	[2]	[3]	This work [15]
Technology	**130nm Bulk**	**32nm Bulk**	**45nm SOI**	**32nm SOI**
Topology	**2/1 step-up**	**2/1 step-up**	**2/1 step-down**	**2/3, 1/2, 1/3 step-down**
Capacitor Technology	**MIM**	**Metal finger**	**Deep trench**	**CMOS oxide**
Interleaved Phases	**16**	**32**	**1**	**32**
C_{out}	**400pF (= C_{fly})**	**0**	**Yes**	**0**
Converter Area	**2.25 mm²**	**6678 µm²**	**1200 µm²**	**0.378 mm² (1.4% used for load)**
Efficiency (η)	**82%**	**60%**	**90%**	**81%**
Power density @ η	**2.09 mW/mm²**	**1.123 W/mm²**	**2.185 W/mm²**	**0.55 W/mm²**

[1] T. Van Breussegem and M. Steyaert, *IEEE Symp. VLSI Circuits,* pp. 198 – 199, June, 2009
[2] D. Somasekhar, et .al, *IEEE J. Solid-State Circuits*, Vol. 45, No. 4, pp. 751 – 758, 2010.
[3] L. Chang, R. Montoye, B. Ji, A. Weger, K. Stawiasz, R. Dennard, *IEEE Symp. VLSI Circuits*, June, 2010

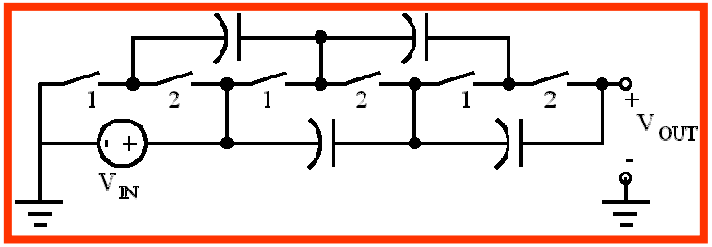
Charts: 2-1 V & 1-2 V functions



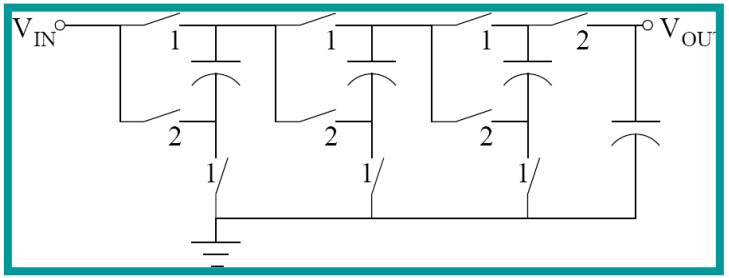


Comparison with Magnetic Designs

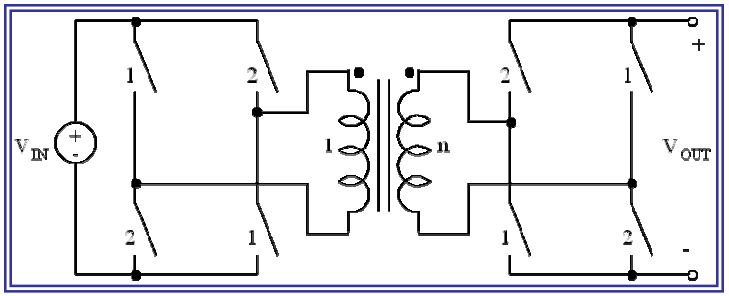
Ladder-type switched-cap converter



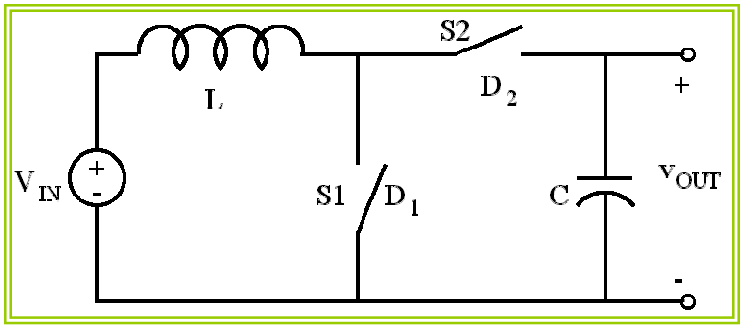
Series-Parallel SC converter



Transformer-bridge converter

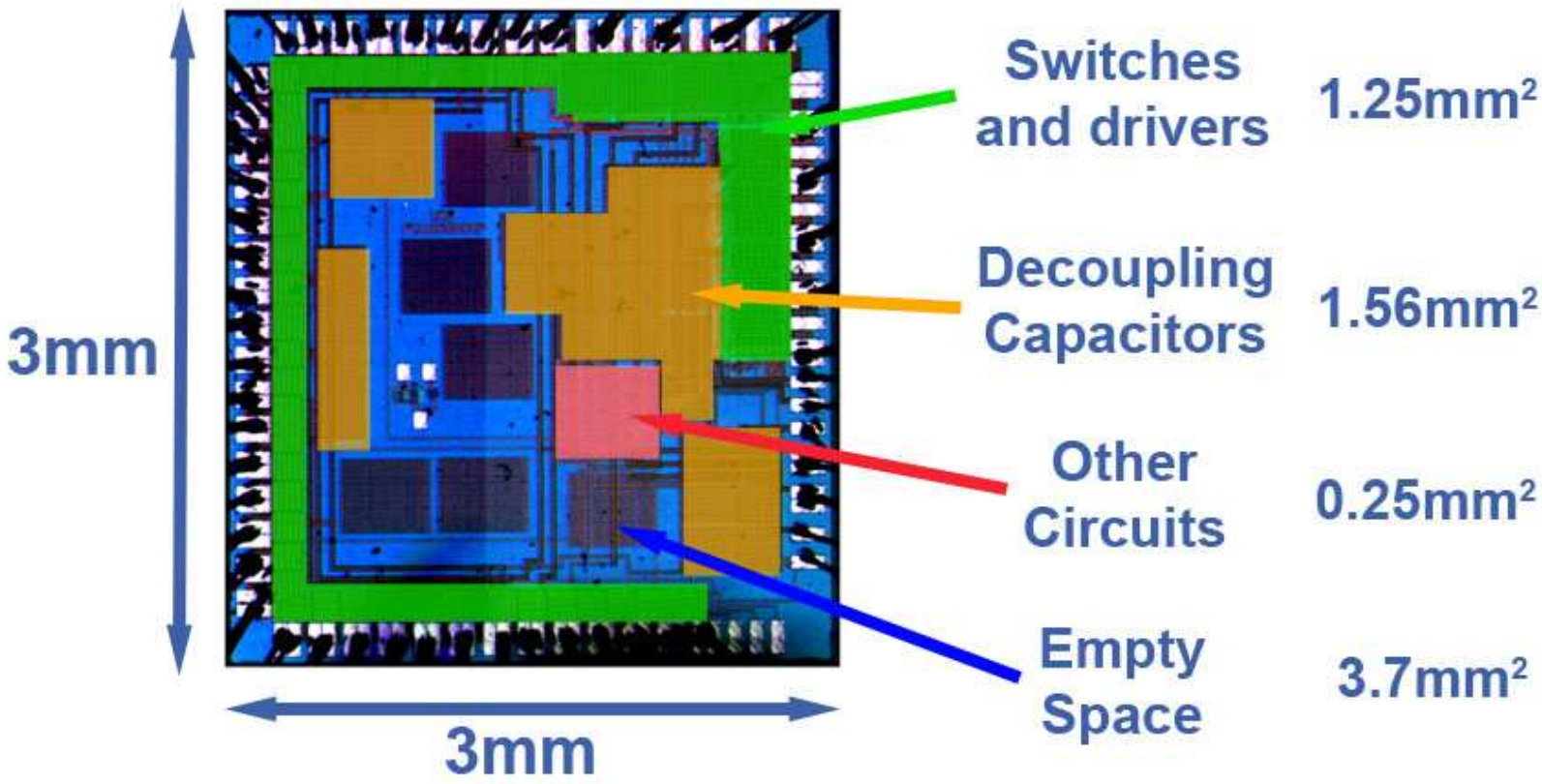


Boost or Buck converter



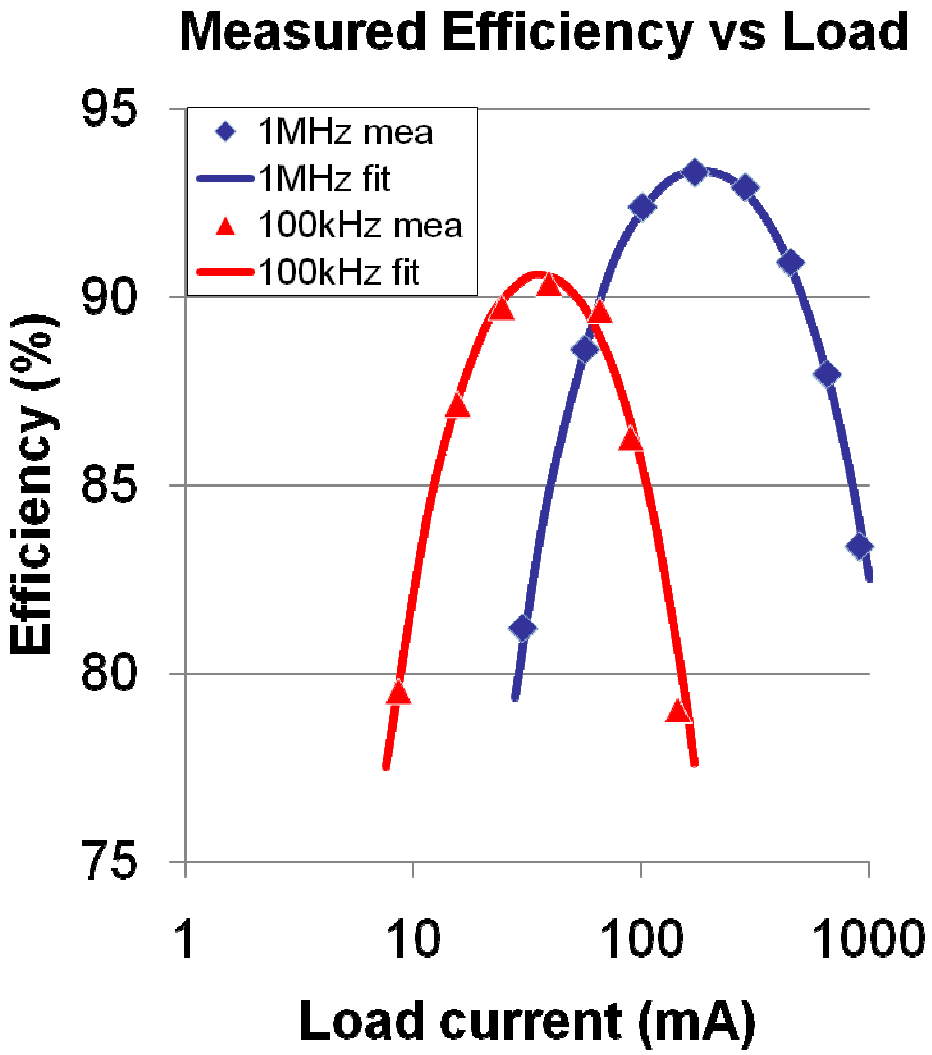
Switch sizes optimized for a given conversion ratio *n* for each converter

Test Chip Layout in Triple-Well 0.18 µm CMOS9



- Switches at periphery and numerous bond-pads and bond-wires are to reduce series resistances
- Solder bump reduces die size

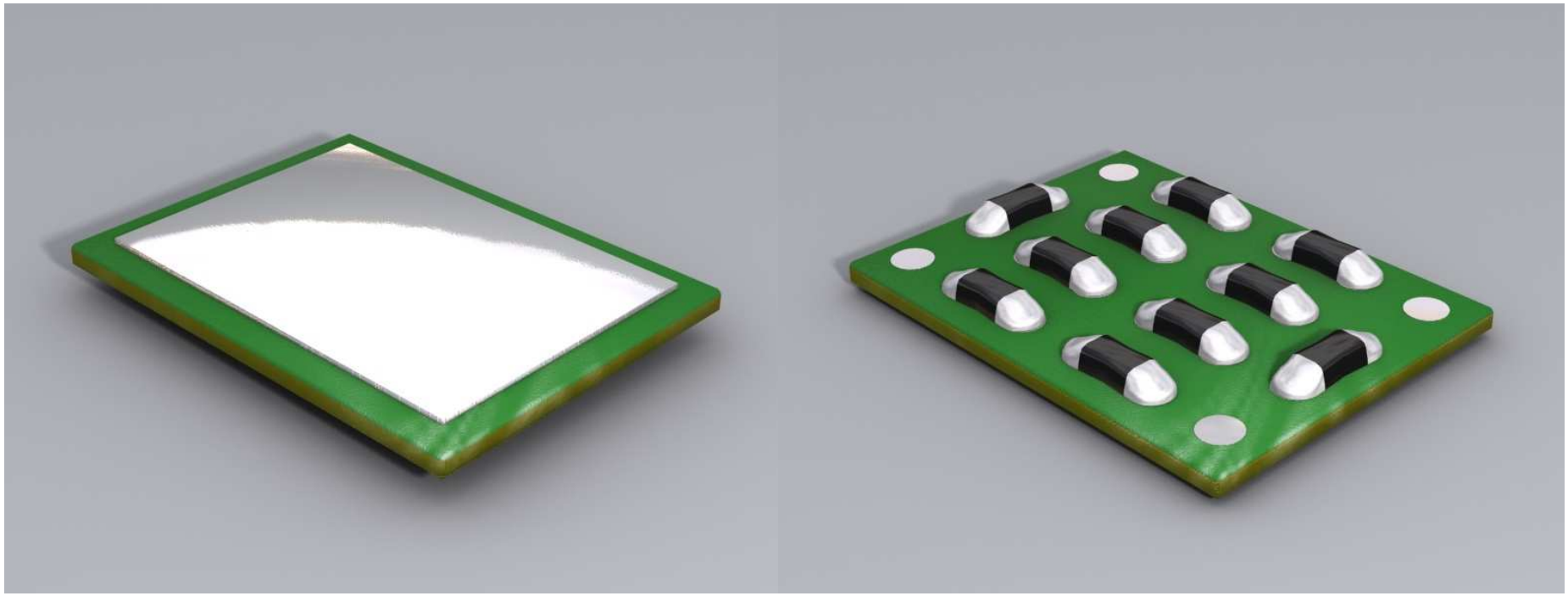
Design vs. Measured Performance



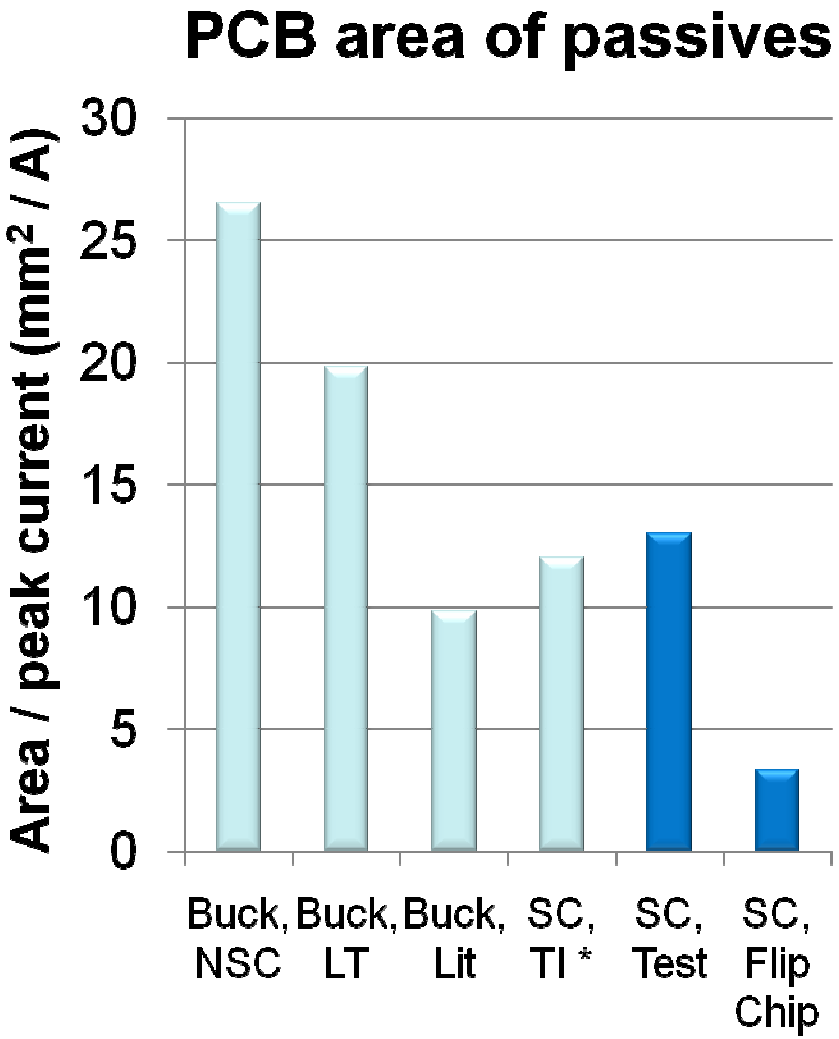
	Design	Est.
R_{OUT}@1MHz	210mΩ	287mΩ
Fixed Loss	0.3mW	2.1mW
Freq-dep Loss	7.5mW	5.5mW
Peak eff	**95%**	**93%**
Eff at 1A	**85%**	**83%**

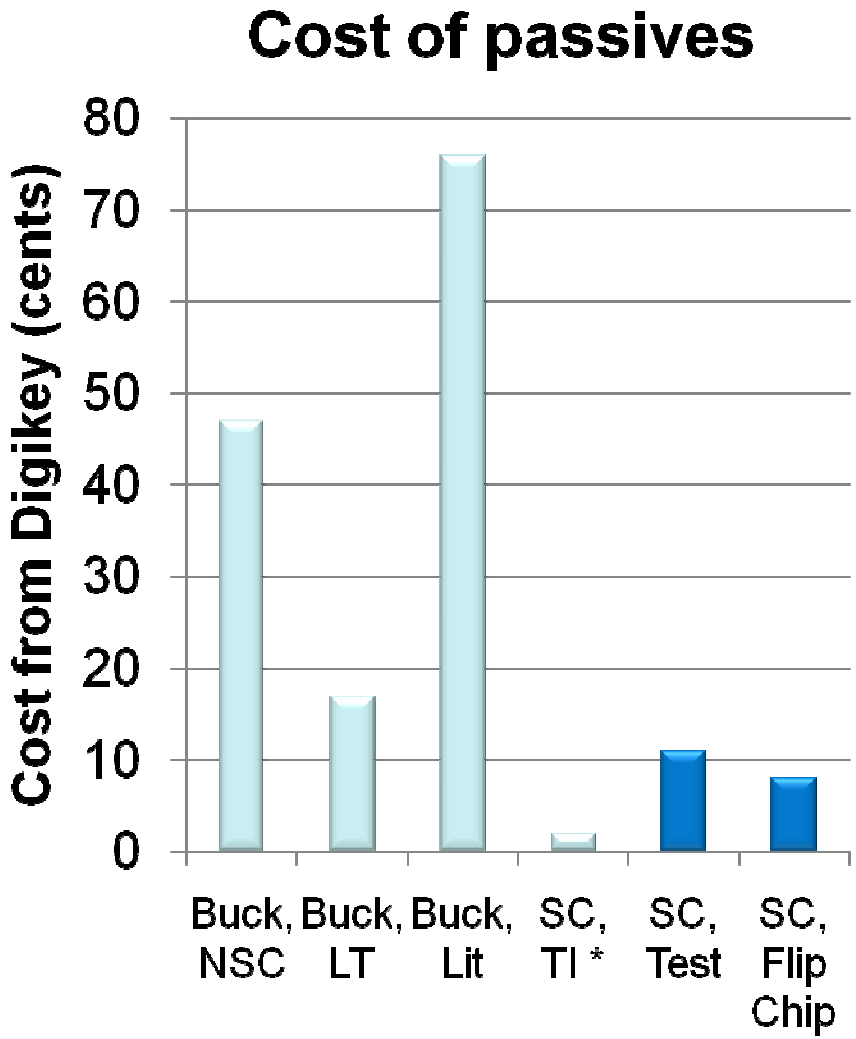
Contribution to R_{FSL}	
All switches	51mΩ
On-chip metal	39mΩ
Capacitor R_{ESR}	15mΩ
Bond-wire	65mΩ

POL Package Concept: Flip Chip Packaging Scheme



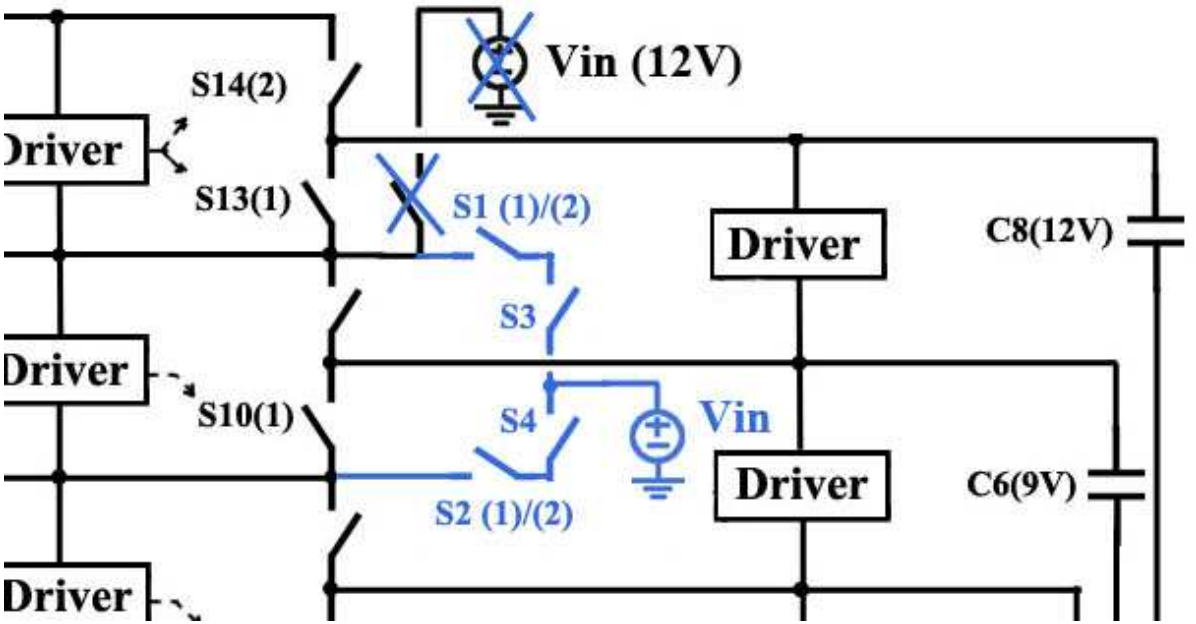
PCB Area and Cost Comparison





* The TI SC has a much lower conversion ratio of 3:1

Regulation



- Regulation can be achieved by
  - Changing switching frequency (SSL), or switch modulation (FSL)
  - Changing conversion ratio
- Circuit in figure supports 4 different conversion ratios
  - By tapping at different nodes of the circuit at different phase

Freq mod state machine

If V_{SG} > 1.3

CLK_{TARGET} = 9 (2.5MHz)

else if V_{SG} > 0.8

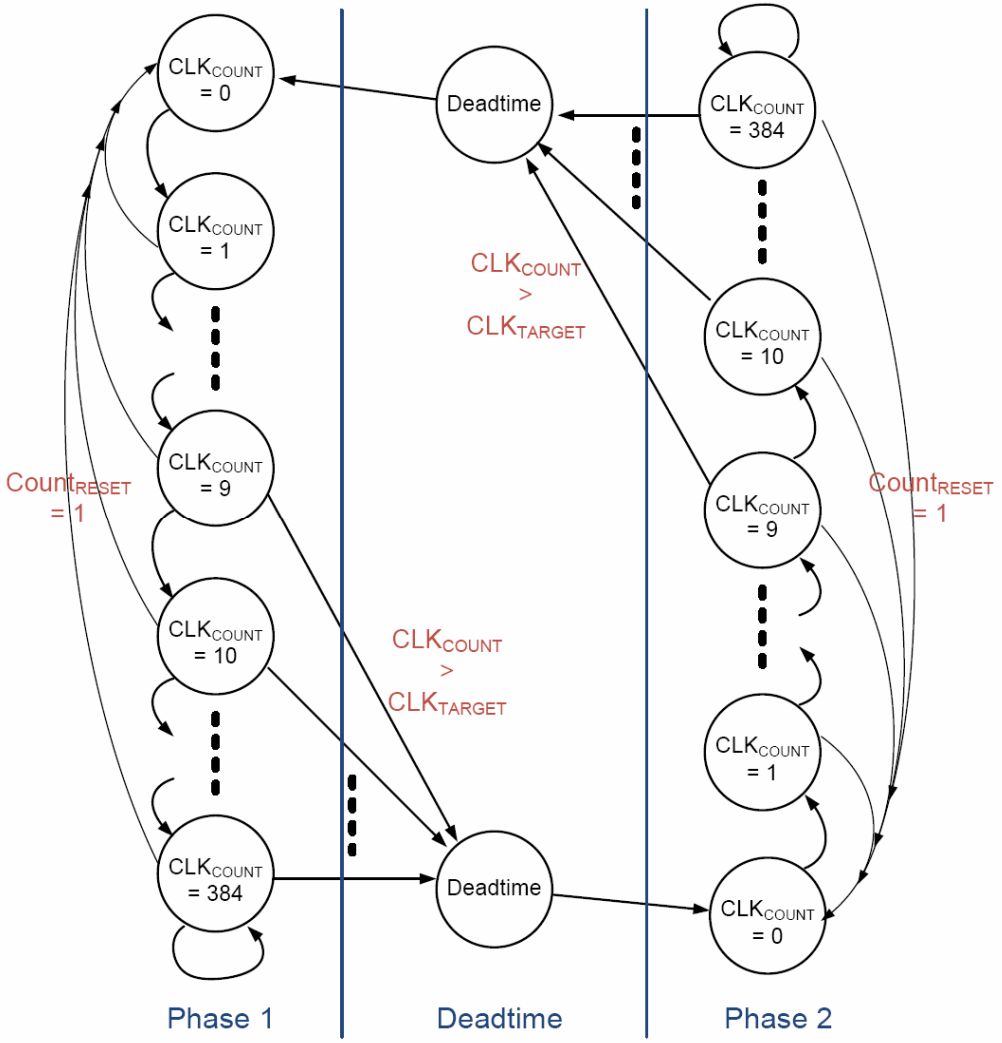
CLK_{TARGET} = 20 (1.25MHz)

else if V_{SG} > 0.6

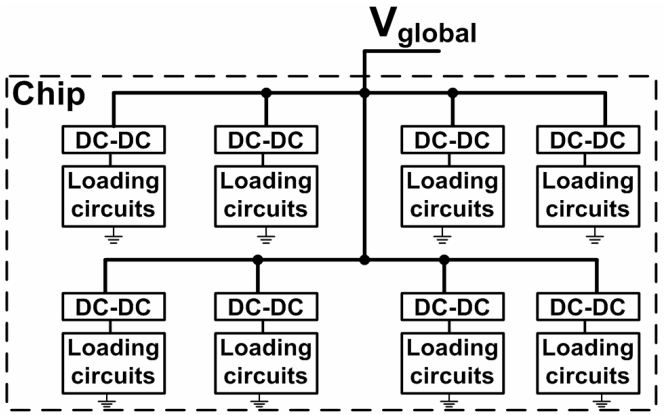
CLK_{TARGET} = 100 (250kHz)

else

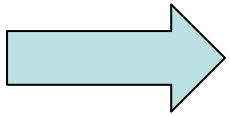
CLK_{TARGET} = 500 (0Hz)

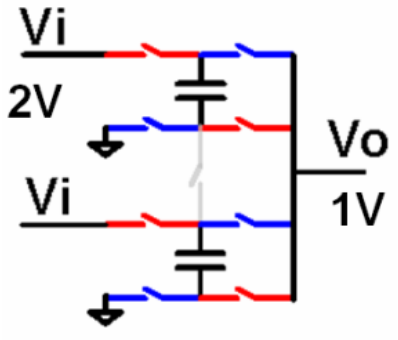


Ex. 1:Fully Integrated Power Delivery for High-Performance Digital ICs



The need





Use fully integrated reconfigurable Switched-Capacitor DC-DC converter

ISSCC 2010

82% Effi. at 0.55W/mm²

3 reconf. topologies